Contents

25 Operational Amplifiers

INTRODUCTION

Historically, an operational amplifier (*OP*-Amp) was designed to perform such mathematical operations as addition, subtraction, integration and differentiation. Hence, the name operational amplifier. An operational amplifier is a multistage amplifier and consists of a differential amplifier stage, a high-gain *CE* amplifier stage and class *B* push-pull emitter follower. An operational amplifier (*OP*-Amp) is an *integrated circuit and is widely used in computers, as video and audio amplifiers in communication electronics. Because of their multi-purpose use, *OP*-Amps are

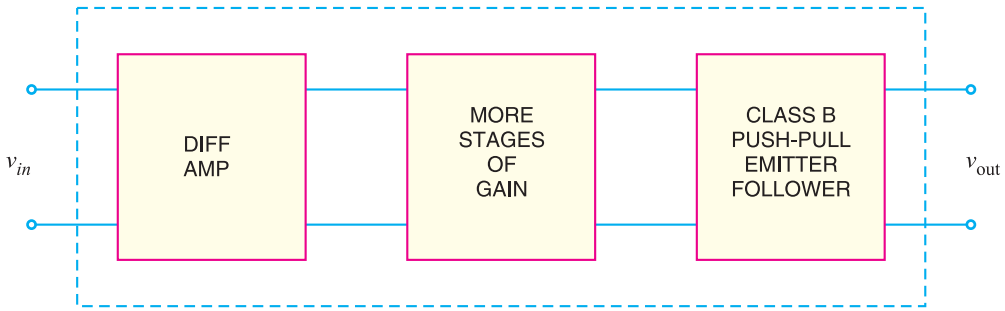
* All the components of an *OP*-Amp (*e.g.*, transistors, resistors etc.) are fabricated on a small chip called integrated circuit.

used in all branches of electronics, both digital and linear circuits. In this chapter, we shall discuss the various aspects of operational amplifiers.

25.1 Operational Amplifier

An **operational amplifier** (*OP-Amp*) *is a circuit that can perform such mathematical operations as addition, subtraction, integration and differentiation.*

Fig. 25.1 shows the block diagram of an operational amplifier. Note that *OP*-Amp is a multistage amplifier. The three stages are : differential amplifier input stage followed by a high-gain *CE* amplifier and finally the output stage. *The key electronic circuit in an OP-Amp is the* **differential amplifier.** A differential amplifier (*DA*) can accept two input signals and amplifies the difference between these two input signals.



Block diagram of OP-Amp

Fig. 25.1

The following points may be noted about operational amplifiers (*OP*-Amps) :

(*i*) The input stage of an *OP*-Amp is a *differential amplifier* (*DA*) and the output stage is typically a class *B* push-pull emitter follower.

(*ii*) The internal stages of an *OP*-Amp are *direct-coupled* *i.e.*, no coupling capacitors are used. The direct coupling allows the *OP*-Amp to amplify d.c. as well as a.c. signals.

(*iii*) An OP-Amp has *very high input impedance* (ideally infinite) and *very low output impedance* (ideally zero). The effect of high input impedance is that the amplifier will draw a very small current (ideally zero) from the signal source. The effect of very low output impedance is that the amplifier will provide a constant output voltage independent of current drawn from the source.

(*iv*) An OP-Amp has *very high *open-loop voltage gain* (ideally infinite); typically more than 200,000.

(*v*) The OP-Amps are almost always operated with negative feedback. It is because the open-loop voltage gain of these amplifiers is very high and we can sacrifice the gain to achieve the advantages of negative feedback including large bandwidth (*BW*) and gain stability (Refer to chapter 13 of the book).

* The gain of an OP-Amp without feedback circuit is called open-loop gain. The gain of an *OP*-Amp with feedback circuit is called closed-loop gain. These terms were discussed in Chapter 13.

25.2 Differential Amplifier (DA)

Since differential amplifier (*DA*) is key to the operation of *OP*-Amp, we shall discuss this circuit in detail. So far in the book we have considered general-purpose amplifiers. In these conventional amplifiers, the signal (generally single input) is applied at the input terminals and amplified output is obtained at the output terminals. However, we can design an amplifier circuit that accepts two input signals and amplifies the difference between these two signals. Such an amplifier is called a **differential amplifier* (*DA*).

A **differential amplifier** *is a circuit that can accept two input signals and amplify the difference between these two input signals.*

Fig. 25.2 shows the block diagram of an ordinary amplifier. The input voltage v is amplified to Av where A is the voltage gain of the amplifier. Therefore, the ouput voltage is $v_0 = Av$.

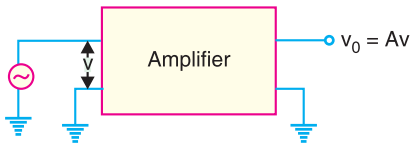


Fig. 25.2

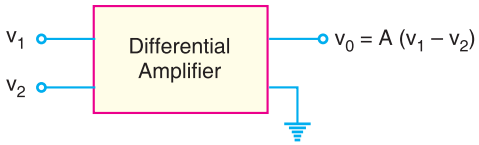


Fig.25.3

Fig. 25.3 shows the block diagram of a differential amplifier. There are two input voltages v_1 and v_2. This amplifier amplifies the difference between the two input voltages. Therefore, the output voltage is $v_0 = A(v_1 - v_2)$ where A is the voltage gain of the amplifier.

Example 25.1. *A differential amplifier has an open-circuit voltage gain of 100. The input signals are 3.25 V and 3.15V. Determine the output voltage.*

Solution.

Output voltage, $v_0 = A(v_1 - v_2)$

Here, $A = 100$; $v_1 = 3.25$ V : $v_2 = 3.15$V

$\therefore \quad v_0 = 100(3.25 - 3.15) =$ **10V**

25.3 Basic Circuit of Differential Amplifier

Fig. 25.4(*i*) shows the basic circuit of a differential amplifier. It consists of two transistors Q_1 and Q_2 that have identical (ideally) characteristics. They share a common positive supply **V_{CC}, common emitter resistor R_E and common negative supply V_{EE}. Note that the circuit is symmetrical. Fig. 25.4(*ii*) shows the symbol of differential amplifier.

The following points may be noted about the differential amplifier :

(*i*) The differential amplifier (*DA*) is a two-input terminal device using atleast two transistors. There are two output terminals marked 1 ($v_{out\ 1}$) and 2($v_{out\ 2}$).

* The name is appropriate because the amplifier is amplifying the difference between the two input signals.

** Note that for this circuit, we need two supply voltages viz. + V_{CC} and –V_{EE}. The negative terminal of V_{CC} is grounded and positive terminal of V_{EE} is grounded.

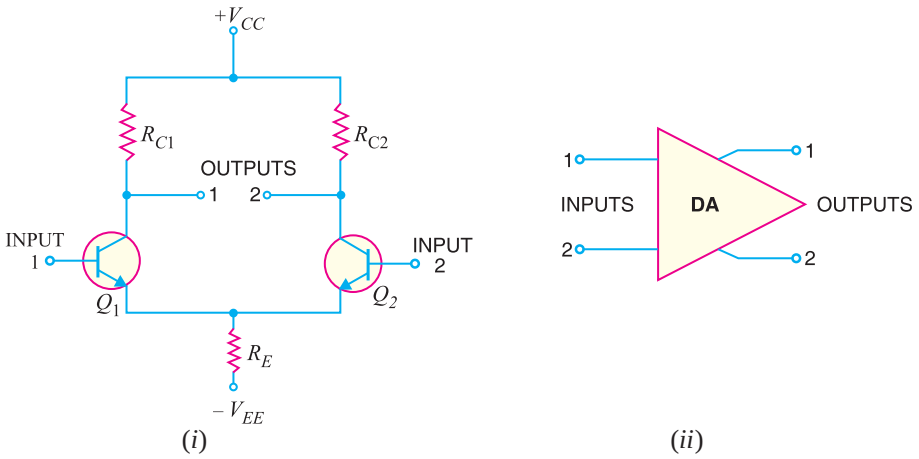


Fig. 25.4

(*ii*) The *DA* transistors Q_1 and Q_2 are matched so that their characteristics are the same. The collector resistors (R_{C1} and R_{C2}) are also equal. The equality of the matched circuit components makes the *DA* circuit arrangement completely symmetrical.

(*iii*) We can apply signal to a differential amplifier (*DA*) in the following two ways :

(*a*) The signal is applied to one input of *DA* and the other input is grounded. In that case, it is called *single-ended input* arrangement.

(*b*) The signals are applied to both inputs of *DA*. In that case, it is called *dual-ended* or *double-ended input* arrangement.

(*iv*) We can take output from *DA* in the following two ways :

(*a*) The output can be taken from one of the output terminals and the ground. In that case, it is called *single-ended output* arrangement.

(*b*) The output can be taken between the two output terminals (*i.e.*, between the collectors of Q_1 and Q_2). In that case, it is called *double-ended output* arrangement or *differential output*.

(*v*) *Generally, the differential amplifier (DA) is operated for single-ended output.* In other words, we take the output either from output terminal 1 and ground or from output terminal 2 and ground. Any input/output terminal that is grounded is at *0V*.

25.4 Operation of Differential Amplifier

For *simplicity, we shall discuss the operation of single-ended input (*i.e.*, signal is applied to one input of *DA* and the other input is grounded) and double-ended output *DA*.

(*i*) Suppose the signal is applied to input 1 (*i.e.*, base of transistor Q_1) and input 2 (*i.e.*, base of transistor Q_2) is grounded as shown in Fig. 25.5. The transistor Q_1 will act in two ways : as a common emitter amplifier and as a common collector amplifier. As a common emitter amplifier, the input signal to Q_1 (input 1) will appear at output 1 (*i.e.*, collector of Q_1) as amplified inverted signal as shown in Fig. 25.5. As a common collector amplifier, the signal appears on the emitter of Q_1 in phase with the input and only slightly smaller. Since the emitters of Q_1 and Q_2 are common, the

* The operation of double-ended input *DA* will then be easier to understand.

emitter signal becomes input to Q_2. Therefore, Q_2 functions as a *common base amplifier. As a result, the signal on the emitter of Q_2 will be amplified and appears on output 2 (*i.e.*, collector of Q_2) in phase with the emitter signal and hence in phase with the input signal (signal at input 1). This is illustrated in Fig. 25.5.

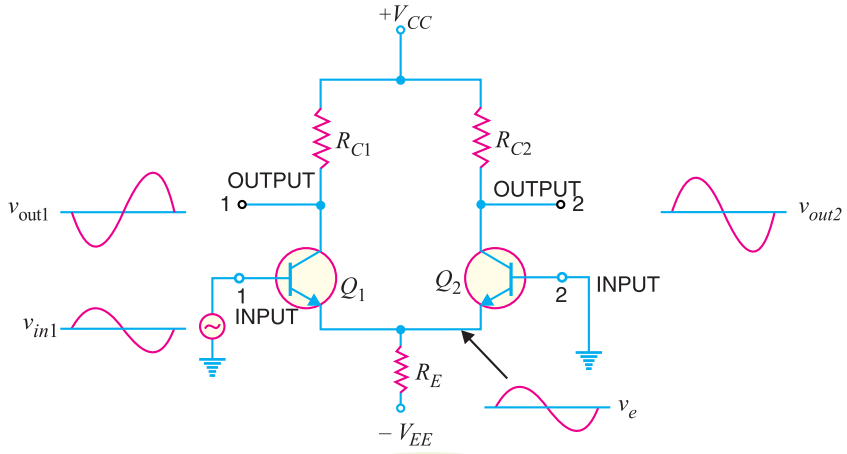


Fig. 25.5

(ii) Now suppose the signal is applied to input 2(*i.e.*, base of transistor Q_2) and input 1(base of transistor Q_1) is grounded. As explained above, now Q_2 acts as a common emitter amplifier and common collector amplifier while Q_1 functions as a common base amplifier. Therefore, an inverted and amplified signal appears at output 2 (*i.e.*, at collector of Q_2) and non-inverted, amplified signal appears at output 1(*i.e.*, at collector of Q_1). This is illustrated in Fig. 25.6.

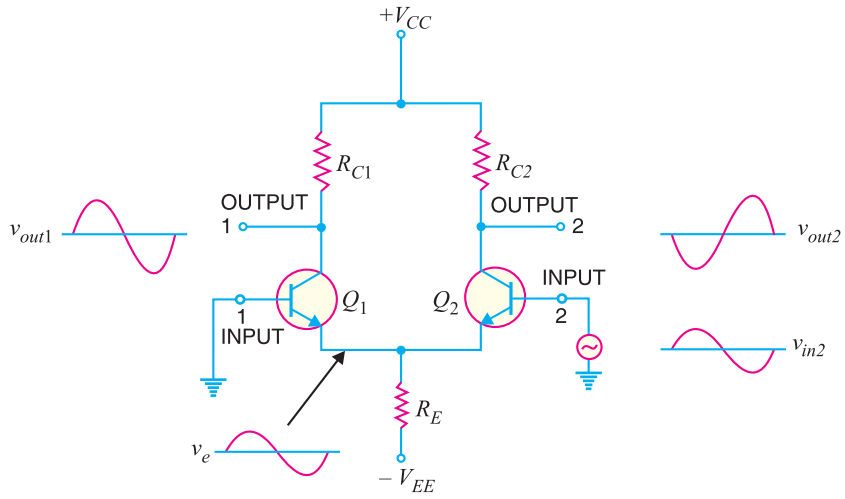


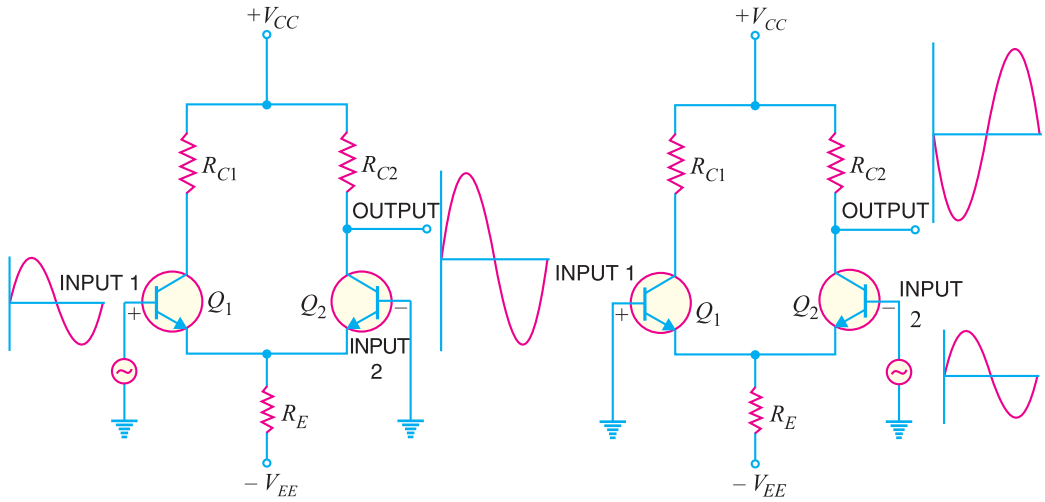
Fig. 25.6

The following points are worth noting about single-ended input *DA* :

(a) When signal is applied to input 1 (*i.e.*, base of transistor Q_1 in Fig. 25.5), an inverted, amplified signal appears at output 1 and non-inverted, amplified signal appears at output 2. Reverse happens when signal is applied to input 2 and input 1 is grounded.

* In a common base amplifier, output signal is in phase with the input signal. Recall that only in *CE* amplifier, the output voltage is 180° out of phase with the input voltage.

(*b*) When only one output terminal is available, the phase of the output of single-ended input *DA* depends on which input receives the input signal. This is illustrated in Fig. 25.7.



(*i*) Noninverting input (*ii*) Inverting input

Fig. 25.7

When signal applied to the input of *DA* produces no phase shift in the output, it is called *non-inverting input* [See Fig. 25.7 (*i*)]. In other words, for noninverting input, the output signal is in phase with the input signal. When the signal applied to the input of *DA* produces 180° phase shift, it is called *inverting input* [See Fig. 25.7 (*ii*)]. In other words, for inverting input, the output signal is 180° out of phase with the input signal. Since inverting input provides 180° phase shift, it is often identified with –sign. The noninverting input is then represented by +*sign. It may be noted that terms noninverting input and inverting input are meaningful when only one output terminal of *DA* is available.

25.5 Common-mode and Differential-mode Signals

The importance of a differential amplifier lies in the fact that the outputs are proportional to the *difference* between the two input signals. Thus the circuit can be used to amplify the difference between the two input signals or amplify only one input signal simply by grounding the other input. The input signals to a *DA* are defined as :

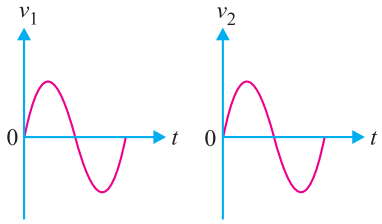
(*i*) Common-mode signals **(*ii*)** Differential-mode signals

(*i*) Common-mode signals : When the input signals to a *DA* are in phase and exactly equal in amplitude, they are called *common-mode signals* as shown in Fig. 25.8. The common-mode signals are rejected (not amplified) by the differential amplifier. It is because a differential amplifier amplifies the difference between the two signals ($v_1 - v_2$) and for common-mode signals, this difference is zero. Note that for common-mode operations, $v_1 = v_2$.

(*ii*) Differential-mode signals. When the input signals to a *DA* are 180° out of phase and exactly equal in amplitude, they are called *differential-mode signals* as shown in Fig. 25.9.

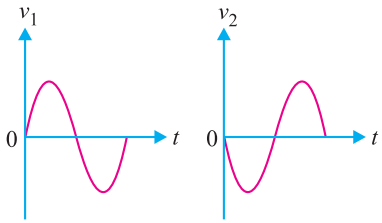
The differential-mode signals are amplified by the differential amplifier. It is because the difference in the signals is twice the value of each signal. For differential-mode signals, $v_1 = -v_2$.

* Note that in Fig. 25.7, the noninverting input terminal is given the +ve sign while the inverting input terminal is given the –ve sign.



Common-mode signals

Fig. 25.8



Differential-mode signals

Fig. 25.9

Thus we arrive at a very important conclusion that a differential amplifier will amplify the differential-mode signals while it will reject the common-mode signals.

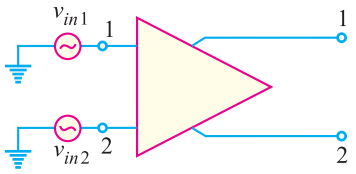
25.6 Double-ended Input Operation of DA

A differential amplifier (*DA*) has two inputs so that it can simultaneously receive two signals. The input signals to a *DA* are defined as :

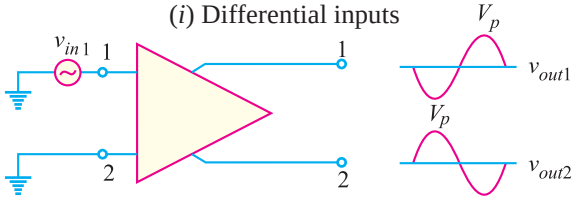
(*i*) Differential-mode signals **(*ii*)** Common-mode signals

The differential-mode signals are equal in amplitude but 180° out of phase. The common-mode signals are equal in magnitude and have the same phase.

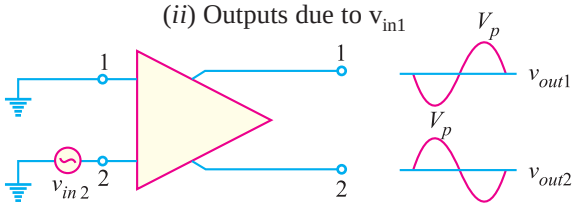
(*i*) Differential input. In this mode (arrangement), two opposite-polarity (180° out of phase) signals are applied to the inputs of *DA* as shown in Fig. 25.10 (*i*).



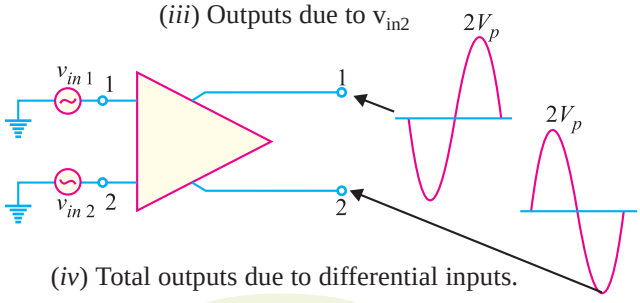
(*i*) Differential inputs



(*ii*) Outputs due to v_{in1}



(*iii*) Outputs due to v_{in2}

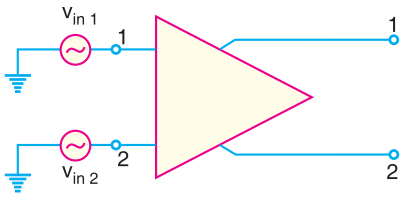


(*iv*) Total outputs due to differential inputs.

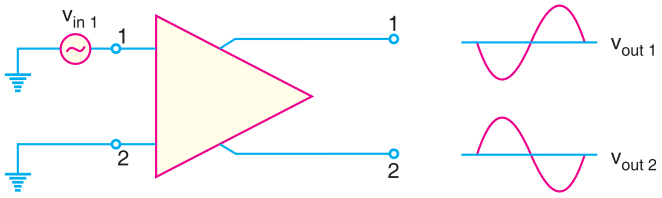
Fig. 25.10

As we shall see, each input affects the *outputs. Fig. 25.10 (*ii*) shows the output signals due to the signal on input 1 acting alone as a single-ended input. Fig. 25.10 (*iii*) shows the output signals due to the signal on **input 2 acting alone as a single-ended input. Note that in Figs. 25.10 (*ii*) and (*iii*), the signals on output 1 are of the same polarity. The same is also true for output 2. By superimposing both output 1 signals and both output 2 signals, we get the total outputs due to differential inputs [See Fig. 25.10(*iv*)].

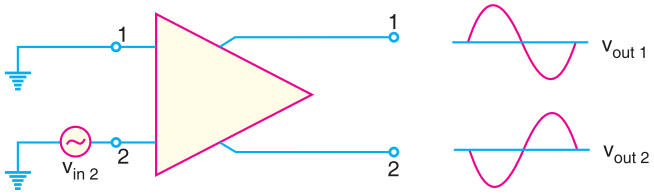
(*ii*) Common-mode input. In this mode, two signals equal in amplitude and having the same phase are applied to the inputs of *DA* as shown in Fig. 25.11(*i*).



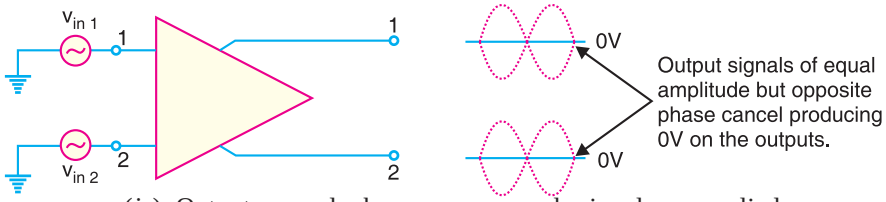
(*i*) Common-mode inputs



(*ii*) Outputs due to v_{in1}



(*iii*) Outputs due to v_{in2}



(*iv*) Outputs cancel when common-mode signals are applied.

Fig. 25.11

* Note that in all the Figures in Fig. 25.10, the phase of the input signal is given in the circle and the phase shift in the output signal is given at the output terminals. Thus in Fig. 25.10 (*ii*), the output signal at terminal 1 is 180° out of phase with the input signal. On the other hand, the output signal at terminal 2 is in phase with the input signal.

** Note that a *DA* amplifies $(v_1 - v_2)$. For Fig. 25.10 (*ii*), $v_{in1} - v_{in2} = v_{in1} - 0 = v_{in1}$. For Fig. 25.10 (*iii*), $v_{in1} - v_{in2} = 0 - v_{in2} = -v_{in2}$.

Again, by considering each input signal acting alone, the basic operation of *DA* in this mode can be explained. Fig. 25.11 (*ii*) shows the output signals due to the signal on only input 1 while Fig. 25.11 (*iii*) shows the output signals due to the signal on only input 2. Note that the corresponding signals on output 1 are of the opposite polarity and so are the ones on output 2. When these are superimposed, they cancel, resulting in zero output voltage as shown in Fig. 25.11 (*iv*).

It is important to note that common-mode signals are rejected by *DA*. This action is called *common-mode rejection.* Most of noises and other unwanted signals are common-mode signals. When these unwanted signals appear on the inputs of a *DA*, they are virtually eliminated on the output.

25.7 Voltage Gains of DA

The voltage gain of a *DA* operating in differential mode is called *differential-mode voltage gain* and is denoted by A_{DM}. The voltage gain of *DA* operating in common-mode is called *common-mode voltage gain* and is denoted by A_{CM}.

Ideally, a *DA* provides a very high voltage gain for differential-mode signals and zero gain for common-mode signals. However, practically, differential amplifiers do exhibit a very small common-mode gain (usually much less than 1) while providing a high differential voltage gain (usually several thousands). The higher the differential gain w.r.t. the common-mode gain, the better the performance of the *DA* in terms of rejection of common-mode signals.

25.8 Common-mode Rejection Ratio (CMRR)

A differential amplifier should have high differential voltage gain (A_{DM}) and very low common-mode voltage gain (A_{CM}). The ratio A_{DM}/A_{CM} is called common-mode rejection ratio (*CMRR*) *i.e.*,

$$CMRR = \frac{A_{DM}}{A_{CM}}$$

Very often, the *CMRR* is expressed in decibels (*dB*). The decibel measure for *CMRR* is given by;

$$CMRR_{dB} = 20\log_{10}\frac{A_{DM}}{A_{CM}} = 20\log_{10} CMRR$$

The following table shows the relation between the two measurements :

CMRR	$CMRR_{dB}$
10	20dB
10^3	60dB
10^5	100dB
10^7	140dB

Importance of CMRR. The *CMRR* is the ability of a *DA* to reject the common-mode signals. The larger the *CMRR*, the better the *DA* is at eliminating common-mode signals. Let us illustrate this point. Suppose the differential amplifier in Fig. 25.12 has a differential voltage gain of 1500 (*i.e.*, A_{DM} = 1500) and a common-mode gain of 0.01 (*i.e.*, A_{CM} = 0.01).

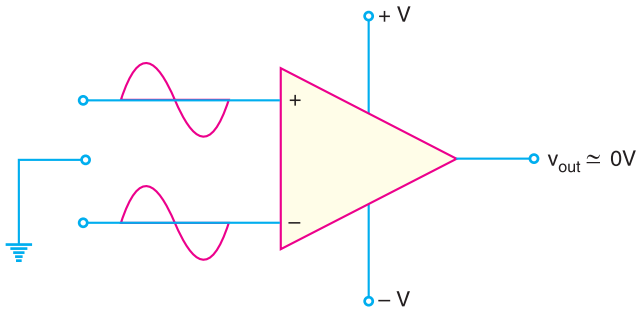


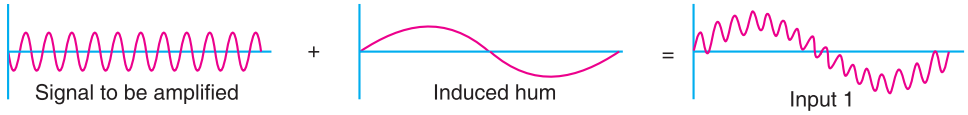
Fig. 25.12

$$\therefore \qquad CMRR = \frac{1500}{0.01} = 150,000$$

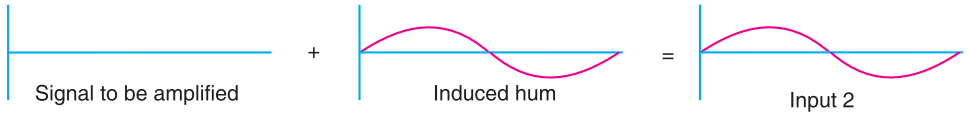
This means that the output produced by a difference between the inputs would be 150,000 times as great as an output produced by a common-mode signal.

The ability of the *DA* to reject common-mode signals is one of its main advantages. Common-mode signals are usually *undesired signals* caused by external interference. For example, any *RF* signals picked up by the *DA* inputs would be considered undesirable. The *CMRR* indicates the *DA*'s ability to reject such unwanted signals.

Practical Illustrations. Fig. 25.13 shows how a differential amplifier (*DA*) rejects hum and static voltages induced into its input leads.



(*i*) Signal input to input 1

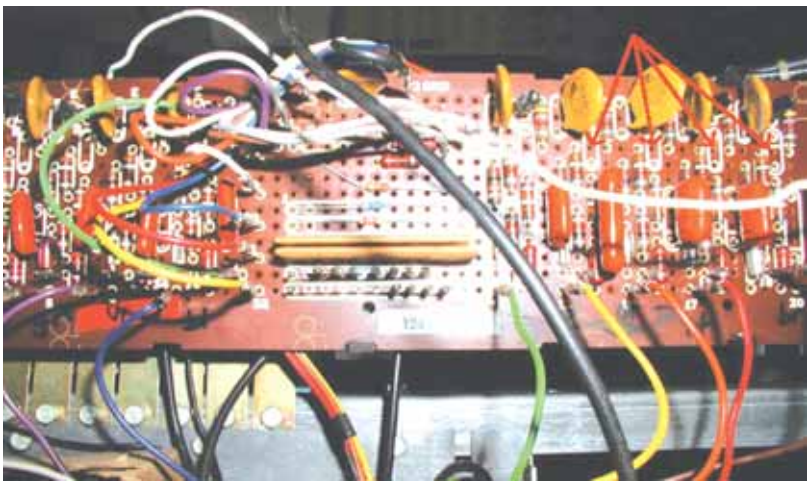


(*ii*) Signal input to input 2

(*iii*) Differential input signal

Fig. 25.13

(i) In Fig. 25.13(*i*), the signal is applied to input 1 of the *DA*. However, a low frequency *hum* voltage is also induced into the lead wire. This hum is produced due to building and collapsing magnetic field generated by adjacent conductor carrying 50Hz current. The resultant waveform is shown in Fig. 25.13 (*i*). If this waveform is amplified by a conventional amplifier, the 50 Hz hum in the output will be stronger than the desired signal.



Low voltage differential amplifier for test and measurement applications.

(*ii*) However, a *DA* also has second input (input 2). Therefore, the lead of second input has the same phase 50 Hz hum induced into it. This is the only voltage (*i.e.*, hum) applied to input 2 as shown in Fig. 25.13(*ii*).

(*iii*) As shown in Fig. 25.13 (*iii*), the hum components of the two inputs form a common-mode signal which is largely rejected by the *DA*. If the input hum signals are equal at the input, then differential input to *DA* will be devoid of hum. Therefore, the amplified output of *DA* will be free from the hum.

Note : We have considered the ideal case *i.e.* $A_{CM} = 0$. Even in a practical case, the value of A_{CM} is less than 1 while A_{DM} is over 200. This means that the desired signal would be over 200 times larger than the hum at the output terminal.

Example 25.2. *A certain differential amplifier has a differential voltage gain of 2000 and a common mode gain of 0.2. Determine CMRR and express it in dB.*

Solution.
$$CMRR = \frac{A_{DM}}{A_{CM}} = \frac{2000}{0.2} = \mathbf{10{,}000}$$
$$CMRR_{dB} = 20 \log_{10} 10{,}000 = \mathbf{80dB}$$

Example 25.3. *A differential amplifier has an output of 1V with a differential input of 10 mV and an output of 5 mV with a common-mode input of 10 mV. Find the CMRR in dB.*

Solution. Differential gain, $A_{DM} = 1\text{V}/10\text{ mV} = 100$

Common-mode gain, $A_{CM} = 5\text{ mV}/10\text{ mV} = 0.5$

$\therefore$ $CMRR_{dB} = 20 \log_{10} (100/0.5) = \mathbf{46\ dB}$

Example 25.4. *A differential amplifier has a voltage gain of 150 and a CMRR of 90 dB. The input signals are 50 mV and 100 mV with 1 mV of noise on each input. Find* (*i*) *the output signal* (*ii*) *the noise on the output.*

Solution.

(*i*) Output signal, $v_{out} = A_{DM}(v_1 - v_2) = 150\ (100\text{ mV} - 50\text{ mV}) = \mathbf{7.5\ V}$

(*ii*) $CMRR_{dB} = 20 \log_{10} (150/A_{CM})$

or $90 = 20 \log_{10} (150/A_{CM})$

$\therefore$ $A_{CM} = 4.7 \times 10^{-3}$

Noise on output $= A_{CM} \times 1\text{ mV} = 4.7 \times 10^{-3} \times 1\text{mV} = \mathbf{4.7 \times 10^{-6}\ V}$

Example 25.5. *The differential amplifier shown in Fig. 25.14 has a differential voltage gain of 2500 and a CMRR of 30,000. A single-ended input signal of 500 μV r.m.s. is applied. At the same time, 1V, 50 Hz interference signal appears on both inputs as a result of radiated pick-up from the a.c. power system.*

(*i*) *Determine the common-mode gain.*

(*ii*) *Express the CMRR in dB.*

(*iii*) *Determine the r.m.s. output signal.*

(*iv*) *Determine the r.m.s. interference voltage on the output.*

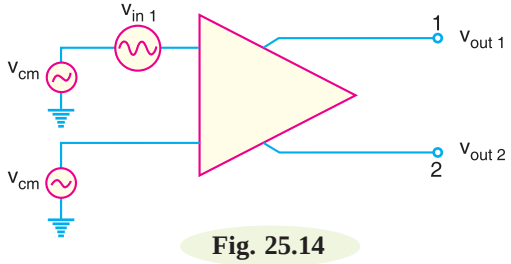


Fig. 25.14

Solution. (*i*) $CMRR = \dfrac{A_{DM}}{A_{CM}}$

$\therefore \quad A_{CM} = \dfrac{A_{DM}}{CMRR} = \dfrac{2500}{30,000} = \mathbf{0.083}$

(*ii*) $CMRR_{dB} = 20 \log_{10} (30{,}000) = \mathbf{89.5\ dB}$

(*iii*) In Fig. 25.14, the differential input voltage is the difference between the voltages on input 1 and that on input 2. Since input 2 is grounded, its voltage is zero.

$\therefore$ Differential input voltage = 500 μV – 0 = 500 μV

The output signal in this case is taken at output 1.

$\therefore \quad v_{out1} = A_{DM} \times (500\ \mu V) = (2500 \times 500)\ \mu V = \mathbf{1.25\ V}$

(*iv*) The common-mode input is 1V r.m.s. and the common-mode gain is $A_{CM} = 0.083$.

$\therefore$ Noise on the output = $A_{CM} \times (1V) = (0.083)\ (1V) = \mathbf{83\ mV}$

25.9 D.C. Analysis of Differential Amplifier (DA)

When no signal is applied to a *DA*, d.c. or quiescent conditions prevail in the circuit. From the transistor circuit theory, we can find *bias voltages and bias currents in the circuit. Fig. 25.15 shows the basic arrangement for an *npn* differential amplifier. Typical circuit values have been assumed to make the treatment illustrative. The circuit is symmetrical *i.e.*, the transistors Q_1 and Q_2 are identical; collector loads are equal ($R_{C1} = R_{C2}$) and base resistors R_B are equal. We assume that base current is very small so that we can ignore the voltage drops across base resistors *i.e.*,

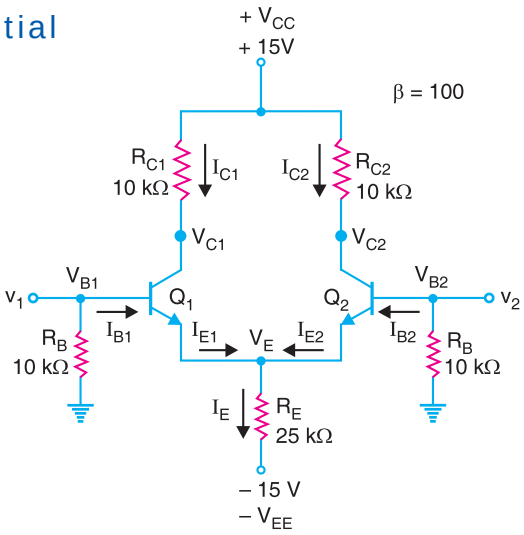


Fig. 25.15

$V_{B1} = V_{B2} \simeq$ **$0V$

Now $V_E = V_{B1} - 0.7 = V_{B2} - 0.7 =$ ***$0 - 0.7 = -0.7$ V

$\therefore \quad V_{E1} = V_{E2} = V_E = \mathbf{-0.7\ V}$

† Voltage across $R_E = V_{EE} - V_{BE}$

Current in R_E, $I_E = \dfrac{V_{EE} - V_{BE}}{R_E}$

---

* Bias voltages and currents mean d.c. values.

** As we shall see, for the considered circuit values, $I_{B1} = I_{B2} = 2.86\ \mu A$.

$\therefore$ Base voltage, $V_B = I_B \times R_B = 2.86\ \mu A \times 10\ k\Omega = 28.6$ mV. Compared to the –15V of V_{EE}, this is a negligible amount of voltage.

*** $V_{BE} = 0.7$ V. There is a plus-to-minus drop in going from the base to emitter. Since base voltage is 0*V*, $V_E = -0.7$ V.

† Applying Kirchhoff's voltage law to the loop consisting of V_{EE}, the base-emitter junction of Q_1 and R_B, we have,

$$V_{RE} = V_{EE} - V_{BE} - V_{RB} = V_{EE} - V_{BE} - 0 = V_{EE} - V_{BE}$$

The current through the emitter resistor R_E is called †**tail current.** For the circuit values considered in Fig.25.15, we have,

$$\text{Tail current, } I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{(15 - 0.7)\text{V}}{25\ \text{k}\Omega} = \mathbf{0.572\ mA}$$

Because of the symmetry in the circuit, I_E must split equally between Q_1 and Q_2.

$$\therefore \quad I_{E1} = I_{E2} = \frac{I_E}{2} = \frac{0.572\ \text{mA}}{2} = \mathbf{0.286\ mA}$$

Now $\quad I_{C1} \simeq I_{E1} = \mathbf{0.286\ mA}$; $I_{C2} \simeq I_{E2} = \mathbf{0.286\ mA}$

Also $\quad I_{B1} = \frac{I_{C1}}{\beta} = \frac{0.286\ \text{mA}}{100} = \mathbf{2.86\ \mu A}$; $I_{B2} = \frac{I_{C2}}{\beta} = \mathbf{2.86\ \mu A}$

$$V_{C1} = V_{CC} - I_{C1} R_{C1} = 15\ \text{V} - 0.286\ \text{mA} \times 10\ \text{k}\Omega = \mathbf{12.1\ V}$$

$$V_{C2} = V_{CC} - I_{C2} R_{C2} = 15\ \text{V} - 0.286\ \text{mA} \times 10\ \text{k}\Omega = \mathbf{12.1\ V}$$

Note that bold type results are bias voltages or bias currents. An important point to see is that $V_{C1} = V_{C2} = 12.1$ V. It means that there is no potential difference between the collectors. Therefore, the differential d.c. output for a balanced *DA* is zero.

Example 25.6. *Find the bias voltages and currents for the differential amplifier circuit shown in Fig. 25.16.*

Solution. Note that there is no resistor in the collector circuit of Q_1. This makes no difference in the values of the two collector currents because the collector currents are determined by the emitter circuit, not the collector circuit. This arrangement will only affect V_{C1}. Because of symmetry in the base-emitter circuits of Q_1 and Q_2, we have,

$$I_{E1} = I_{E2} = \frac{I_E}{2}$$

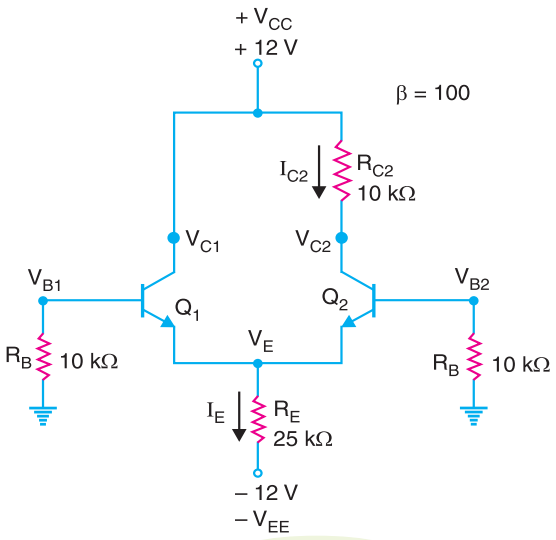


Fig. 25.16

Ignoring the base current, the emitter voltage for both transistors is $V_E = \mathbf{-0.7\ V.}$

Now, $\quad \text{Tail current, } I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{(12 - 0.7)V}{25\ \text{k}\Omega} = \mathbf{0.452\ mA}$

$$\therefore \quad I_{E1} = I_{E2} = I_E/2 = 0.452\ \text{mA}/2 = \mathbf{0.226\ mA}$$

† If you look at the circuit, you can see that emitter resistor R_E is like a tail.

Now, $I_{C1} = I_{C2} = \mathbf{0.226\ mA}$ ($\because I_{C1} \simeq I_{E1}$ and $I_{C2} \simeq I_{E2}$)

$\therefore$ $I_{B1} = I_{B2} = 0.226\ \text{mA}/\beta = 0.226\ \text{mA}/100 = \mathbf{2.26\ \mu A}$

$V_{C1} = V_{CC} = \mathbf{12V}$; $V_{C2} = V_{CC} - I_{C2}R_{C2} = 12 - 0.226\ \text{mA} \times 10\ \text{k}\Omega = \mathbf{9.7V}$

Example 25.7. *In Fig. 25.17, the transistors are identical with β_{dc} = 100. Find the output voltage.*

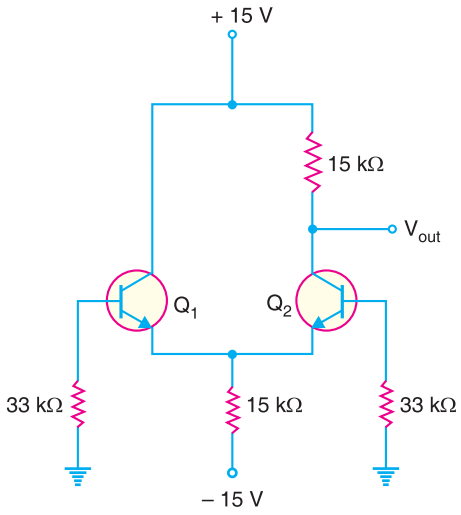


Fig. 25.17

Solution. Tail current, $I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{(15 - 0.7)V}{15\ \text{k}\Omega} = 0.953\ \text{mA}$

Since the transistors are identical, the tail current I_E splits equally between the two transistors. Therefore, emitter current of each transistor = 0.953 mA/2 = 0.477 mA.

Since $I_C \simeq I_E = 0.477\ \text{mA}$, $V_{out} = V_{CC} - I_C R_C = 15 - 0.477\ \text{mA} \times 15\ \text{k}\Omega = \mathbf{7.85\ V}$

Example 25.8. *In Fig. 25.17, the transistors are identical except for β_{dc}. The left transistor has β_{dc} = 90 and the right transistor has β_{dc} = 110. Find (i) base currents (ii) base voltages. Assume V_{BE} = 0V.*

Solution. **(*i*)** Tail current, $I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{(15 - 0)V}{15\ \text{k}\Omega} = 1\text{mA}$

Therefore, the emitter current in each transistor = 1/2 = 0.5 mA.

The base current in the left transistor is

$$I_{B1} = 0.5\ \text{mA}/90 = \mathbf{5.56\ \mu A}$$

The base current in the right transistor is

$$I_{B2} = 0.5\ \text{mA}/110 = \mathbf{4.55\ \mu A}$$

(*ii*) Voltage on left base, $V_{B1} = -$*$(5.56\ \mu\text{A}) \times (33\ \text{k}\Omega) = \mathbf{-0.183\ V}$

Voltage on right base, $V_{B2} = -(4.55\ \mu\text{A}) \times (33\ \text{k}\Omega) = \mathbf{-0.15\ V}$

Since the transistors are not identical, the base currents and base voltages are different.

Example 25.9. *Most differential amplifiers are biased with a current source as shown in Fig. 25.18. Find the bias currents and voltages.*

. . . . . .

* Note that for the ideal case, emitter of each transistor is at 0V.

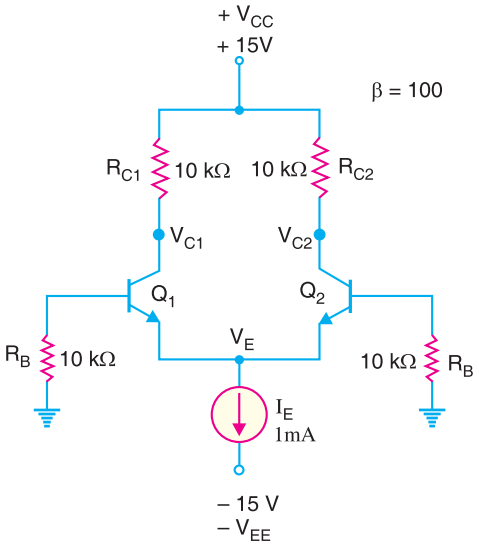


Fig. 25.18

Solution. In this circuit, the current I_E is given by the current source. Ignoring base current, the potential at each emitter is V_E = **–0.7 V.**

Emitter current in each transistor = $I_E/2$ = 1mA/2 = **0.5 mA**

Also $I_{C1} \simeq I_{E1}$ = **0.5 mA** ; $I_{C2} \simeq I_{E2}$ = **0.5 mA**

$\therefore$ $V_{C1} = V_{C2}$ = 15 – 0.5 mA × 10 kΩ = **10V**

Example 25.10. *Fig. 25.19 shows a differential amplifier constructed with pnp transistors. Find the bias currents and voltages.*

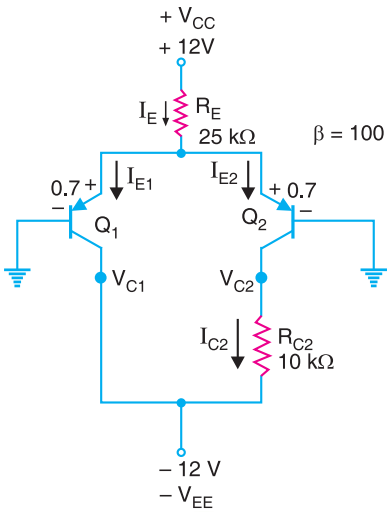


Fig. 25.19

Solution. For the *pnp* transistor, the emitter voltage (V_E) is a diode drop above the base voltage. Therefore, V_E = **+ 0.7 V.**

$$\text{Tail current, } I_E = \frac{V_{CC} - V_E}{R_E} = \frac{(12 - 0.7)V}{25\ \text{k}\Omega} = \textbf{0.452 mA}$$

Current in each emitter of transistor = 0.452 mA/2 = **0.226 mA**

Now, $I_{C1} \simeq I_{E1} = \mathbf{0.226\ mA}$ and $I_{C2} \simeq I_{E2} = \mathbf{0.226\ mA}$

$V_{C1} = -V_{EE} = \mathbf{-12V}$; $V_{C2} = -V_{EE} + I_{C2} R_{C2} = -12 + 0.226\ \text{mA} \times 10\ \text{k}\Omega = \mathbf{-9.74\ V}$

25.10 Overview of Differential Amplifier

Fig. 25.20 shows double-ended input and single-ended output differential amplifier (*DA*). In other words, there are two input signals and one output signal. *A DA is *normally operated in this fashion.* When input signal v_1 (input 1) is applied, the output signal is in phase with the input signal *i.e.*, there is no phase shift in the output signal. For this reason, input signal v_1 is called *non-inverting input*. When input signal v_2 (input 2) is applied, the output signal is 180° out of phase with the input signal. For this reason, input signal v_2 is called *inverting input*.

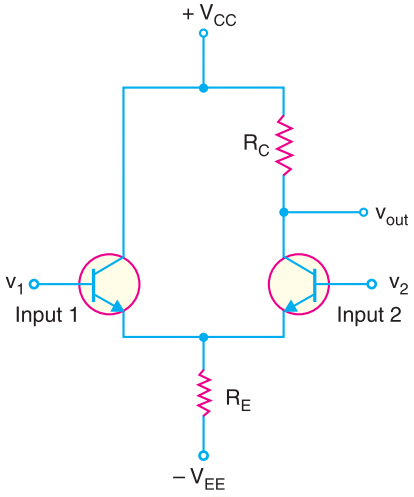


Fig. 25.20

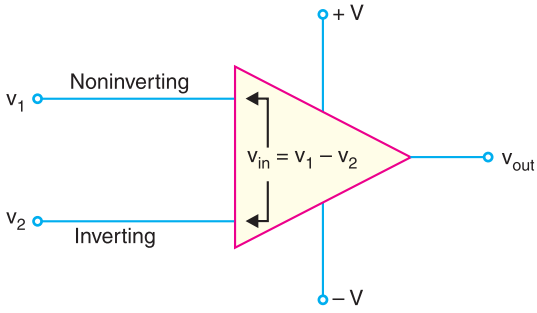


Fig. 25.21

The differential amplifier amplifies the difference between the two input voltages. This point is illustrated in Fig. 25.21. The difference between the input voltages is $v_{in} = v_1 - v_2$ *i.e.*,

$$v_{in} = v_1 - v_2$$

where
v_1 = the voltage applied to the noninverting input
v_2 = the voltage applied to the inverting input
v_{in} = the difference voltage that will be amplified

It is important to remember that the differential amplifier is amplifying the difference between the input terminal voltages.

25.11 Parameters of DA (or OP–amp) due to Mismatch of Transistors

Our discussion on the differential amplifier (*DA*) has been based on the assumption that the transistors are *perfectly matched i.e.*, they have exactly the same electrical characteristics. In practice, this cannot happen. There will always be *some* difference between the characteristics of the two transistors. This leads us to the following two parameters of *DA* (or *OP*– amp) :

1. Output offset voltage **2.** Input offset current

1. Output Offset Voltage. Even though the transistors in the differential amplifier are very closely matched, there are some differences in their electrical characteristics. One of these differences is found in the values of V_{BE} for the twso transistors. When $V_{BE1} \neq V_{BE2}$, an imbalance is created in the differential amplifier. The *DA* (or *OP*-amp) may show some voltage at the output

* One input can be grounded (*i.e.*, at 0V).

even when the voltage applied between two input terminals is zero. This is called *output offset voltage*. This point is illustrated in Fig. 25.22. Note that with the inputs of *DA* grounded, the output shows a measurable voltage. This voltage is a result of the imbalance in the differential amplifier, which causes one of the transistors to conduct harder than the other.

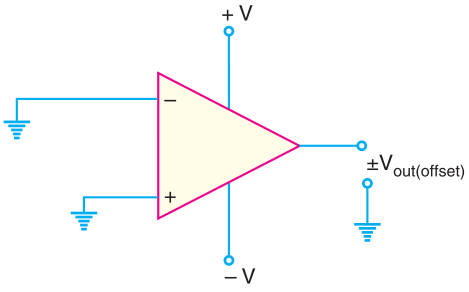


Fig. 25.22

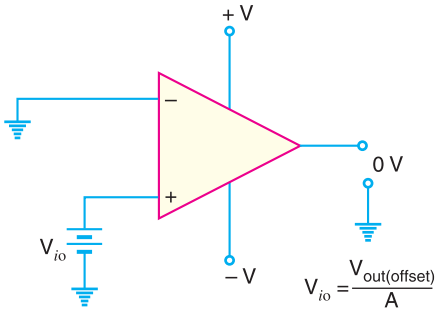


Fig. 25.23

There are several methods that may be used to eliminate output offset voltage. One of these is to apply an *input offset voltage* between the input terminals of *DA* (or *OP*- amp) so as to make output 0*V* as shown in Fig. 25.23. The value of input offset voltage (V_{i0}) required to eliminate the output offset voltage is given by;

$$V_{i0} = \frac{V_{out}(offset)}{A}$$ ...*A* is voltage gain.

2. Input Offset Current. When the output offset voltage of a *DA* (or *OP*- amp) is eliminated, there will be a slight difference between the input currents to the noninverting and inverting inputs of the device. This slight difference in input currents is called *input offset current* and is caused by a beta (β) mismatch between the transistors in the differential amplifier. As an example, suppose I_{B1} = 75 μA and I_{B2} = 65 μA. Then,

$$I_{in\ (offset)} = 75 - 65 = 10\ \mu A$$

The difference in the base currents indicates how closely matched the transistors are. If the transistors are identical, the input offset current is zero because both base currents will be equal. But in practice, the two transistors are different and the two base currents are not equal.

25.12 Input Bias Current

The inputs to an OP- amp require some amount of d.c. biasing current for the transistors in the differential amplifier. The *input bias current* is defined as the average of the two d.c. base currents *i.e.*,

$$I_{in(bias)} = \frac{I_{B1} + I_{B2}}{2}$$

For example, if I_{B1} = 85 μA and I_{B2} = 75 μA, then the input bias current is

$$I_{in(bias)} = \frac{85 + 75}{2} = 80\mu A$$

This means that when no signal is applied, the inputs of *OP*- amp (*i.e.*, *DA*) will draw a d.c. current of 80 μA.

The fact that both transistors in the differential amplifier require an input biasing current leads to the following operating restriction : *An OP- amp will not work if either of its inputs is open.* For example, look

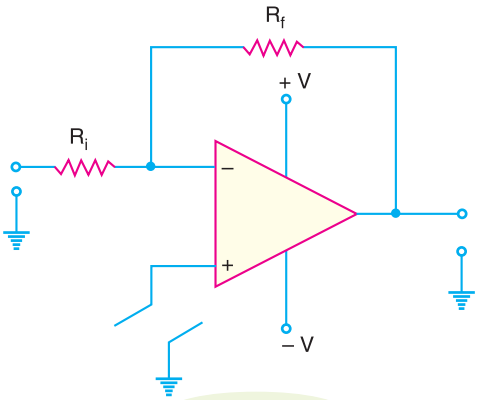


Fig. 25.24

at the circuit shown in Fig. 25.24. The *non-inverting input is shown to have an open between the OP- amp and ground. The open circuit would not allow the d.c. biasing current required for the operation of the differential amplifier (*The transistor associated with the inverting input would work but not the one associated with the non-inverting input*). Since the differential amplifier would not work, the overall *OP*-amp circuit would not work. Thus an input bias current path must always be provided for *both OP*-amp inputs.

Example 25.11. *In Fig. 25.25, the left transistor has* $\beta_{dc} = 90$ *and the right transistor has* $\beta_{dc} = 110$. *Find* (*i*) *the input offset current* (*ii*) *input bias current. Neglect* V_{BE}.

Solution.

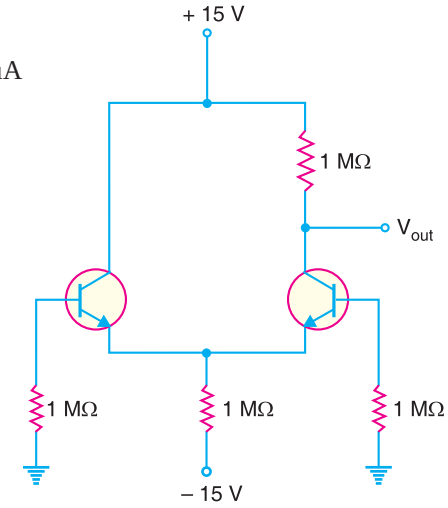


Fig. 25.25

(*i*) Tail current, $I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{(15-0)V}{1\,M\Omega} = 15\ \mu A$

The emitter current in each transistor is

$$I_{E1} = I_{E2} = I_E/2 = 15\mu A/2 = 7.5\ \mu A$$

The base current in the left transistor is

$$I_{B1} = \frac{I_{E1}}{\beta} = \frac{7.5\,\mu A}{90} = 83.3\ nA$$

The base current in the right transistor is

$$I_{B2} = \frac{I_{E2}}{\beta} = \frac{7.5\,\mu A}{110} = 68.2\ nA$$

$\therefore$ Input offset current is given by;

$$I_{in(offset)} = I_{B1} - I_{B2} = 83.3 - 68.2 = \mathbf{15.1\ nA}$$

(*ii*) The input bias current is the average of the two base currents.

$\therefore$ Input bias current, $I_{in(bias)} = \dfrac{I_{B1} + I_{B2}}{2} = \dfrac{83.3 + 68.2}{2} = \mathbf{75.8\ nA}$

Example 25.12. *The data sheet of an IC OP-amp gives these values :* $I_{in(offset)} = 20$ *nA and* $I_{in(bias)} = 80$ *nA. Find the values of two base currents.*

Solution. An $I_{in(offset)}$ of 20 nA means that one base current is 20 nA greater than the other. There is no way to tell which of the two base currents will be greater. It can go either way in mass production. Assume that I_{B1} is greater than I_{B2}. Then,

$$I_{B1} = I_{in(bias)} + \frac{I_{in(offset)}}{2} = 80\ nA + \frac{20nA}{2} = \mathbf{90\ nA}$$

$$I_{B2} = I_{in(bias)} - \frac{I_{in(offset)}}{2} = 80\ nA - \frac{20nA}{2} = \mathbf{70\ nA}$$

If I_{B2} is greater than I_{B1}, then the values are reversed *i.e.*, $I_{B1} = 70$ nA and $I_{B2} = 90$ nA.

Example 25.13. *In Fig. 25.26, what is the output offset voltage if* $I_{in(bias)} = 80$ *nA and* $I_{in(offset)} = 20$ *nA? Assume that voltage gain is* $A = 150$. *Assume only* β_{dc} *differences exist.*

Solution. The two base resistors are equal ; each being 100 kΩ.

$\therefore$ Input offset voltage, $V_{i0} = I_{in(offset)} \times R_B = (20\ nA)\ (100\ k\Omega) = 2\ mV$

$\therefore$ Output offset voltage, $V_{out\ (offset)} = A \times V_{i0} = 150 \times 2\ mV = \mathbf{0.3\ V}$

* Recall that +sign indicates noninverting input and –sign indicates inverting input.

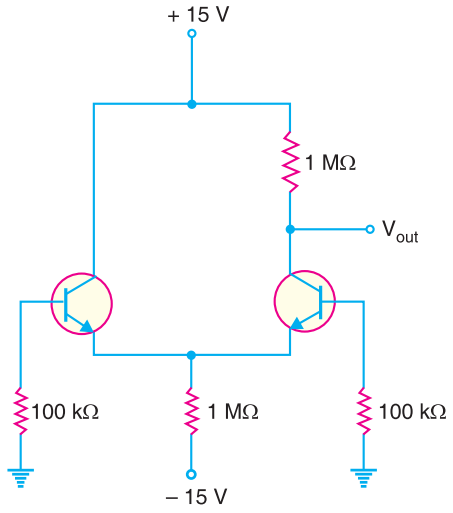


Fig. 25.26

25.13 A.C. Analysis of Differential Amplifier

A differential amplifier (*DA*) has a noninverting input and an inverting input. Fig. 25.27 shows the differential amplifier (*DA*) that is used in *IC OP*- amps. Note the circuit has double-ended input and single-ended output.

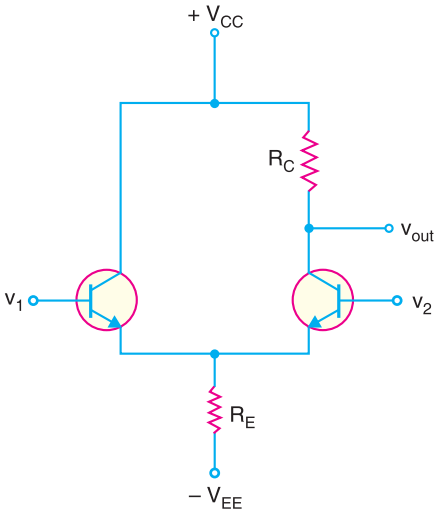


Fig. 25.27

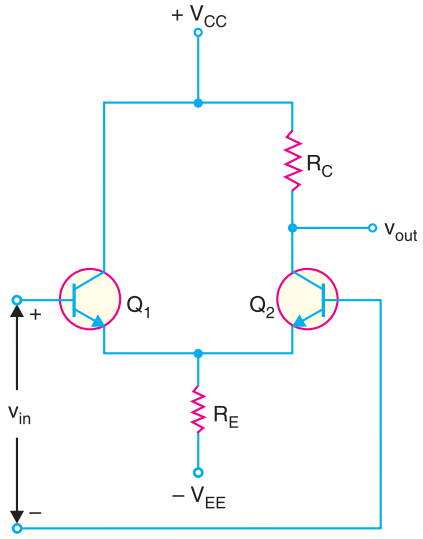


Fig. 25.28

If you look at the differential amplifier circuit in Fig. 25.27, it responds to the difference between the voltages at the two input terminals. In other words, *DA* responds to v_{in} $(= v_1 - v_2)$. Therefore, the circuit shown in Fig. 25.27 can be drawn as shown in Fig. 25.28.

Ideally (*i.e.*, V_{BE} is negligible), the tail current I_E in Fig. 25.27 is $I_E = V_{EE}/R_E$. Once the values of V_{EE} and R_E are set, the tail current is constant. Therefore, to simplify a.c. analysis, we can replace the tail current by a current source (I_E) as shown in Fig. 25.29. This will simplify the a.c. analysis of the circuit with almost no loss of accuracy.

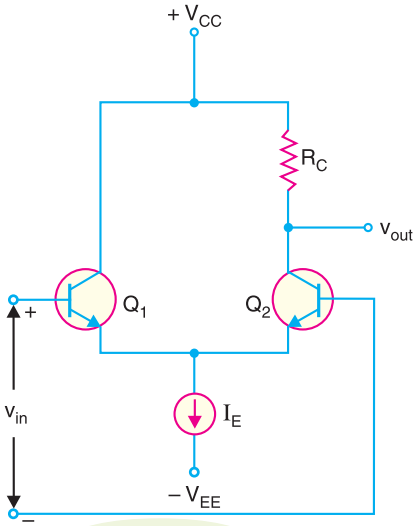


Fig. 25.29

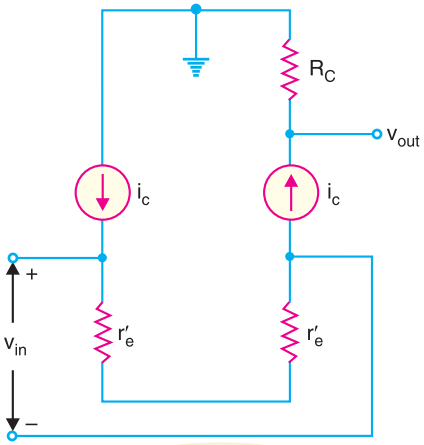


Fig. 25.30

A.C. Equivalent Circuit. We can easily find the a.c. equivalent circuit of differential amplifier by applying the usual rules to Fig. 25.29. The rules are to short all the capacitors, and reduce all d.c. sources to zero. Since a differential amplifier has no capacitors, all that we have to do is to reduce the d.c. sources to zero. Reducing a voltage source to zero is equivalent to replacing it by a short. Reducing a current source to zero is equivalent to opening it. In Fig. 25.29, this means ground the V_{CC} point, ground the V_{EE} point and open the current source. Applying these conditions to Fig. 25.29, we get the a.c. equivalent circuit of differential amplifier shown in Fig. 25.30.

Voltage gain. Fig. 25.30 shows the a.c. equivalent circuit of a differential amplifier. This is how a differential amplifier looks to an a.c. signal. Note that r'_e (= 25 mV/d.c. emitter current) is the a.c. emitter resistance. Since the two r'_es are in series, the same a.c. emitter current exists in both transistors. The a.c. emitter current is given by;

$$i_e = \frac{v_{in}}{2r'_e}$$

This expression is easy to remember because it is almost identical to a *CE* amplifier where $i_e = v_{in}/r'_e$. The only difference is the factor 2 because a differential amplifier uses two transistors.

The a.c. collector current is approximately equal to the a.c. emitter current *i.e.* $i_c \simeq i_e$.

$$\therefore \quad \text{Output voltage, } v_{out} = i_c R_C = \frac{v_{in}}{2r'_e} R_C \qquad \left[\because i_e \simeq i_c = \frac{v_{in}}{2r'_e}\right]$$

$$\therefore \quad \text{Voltage gain, } A = \frac{v_{out}}{v_{in}} = \frac{R_C}{2r'_e}$$

This gain of *DA* is referred to as differential-mode voltage gain and is usually denoted by A_{DM}.

$$\therefore \quad \text{Differential voltage gain, } A_{DM} = \frac{R_C}{2r'_e}$$

Input impedance. The a.c. emitter current is given by;

$$i_e = \frac{v_{in}}{2r'_e} \simeq \beta\, i_b \qquad (\because i_c = \beta i_b \simeq i_e)$$

$$\therefore \quad \frac{v_{in}}{i_b} = 2\beta r_e'$$

Now i_b is the a.c. input current to the differential amplifier. Therefore, v_{in}/i_b is the input impedance.

$$\therefore \quad \text{Input impedance, } Z_i = 2\beta r_e'$$

Example 25.14. *What is v_{out} in Fig. 25.31 when (i) $v_{in} = 1mV$ (ii) $v_{in} = -1mV$?*

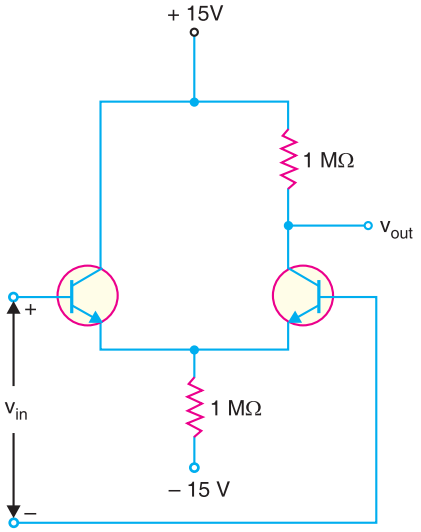


Fig. 25.31

Solution. The ideal tail current, $I_E = V_{EE}/R_E = 15V/1M\Omega = 15\ \mu A$. Therefore, d.c. emitter current in each transistor = $I_{E1} = I_{E2} = I_E/2 = 15\ \mu A/2 = 7.5\ \mu A$.

$$\therefore \quad \text{a.c. emitter resistance, } r_e' = \frac{25\ mV}{I_{E1} \text{ or } I_{E2}} = \frac{25\ mV}{7.5\ \mu A} = 3.33\ k\Omega$$

$$\therefore \quad \text{Differential voltage gain, } A_{DM} = \frac{R_C}{2r_e'} = \frac{1\,M\Omega}{2 \times 3.33\ k\Omega} = 150$$

(i) Output voltage = $A_{DM} \times v_{in} = 150 \times (1mV) = 150\ mV =$ **0.15 V**

(ii) Output voltage, $v_{out} = A_{DM} \times v_{in} = 150 \times (-1\ mV) =$ **– 0.15 V**

Example 25.15. *For the circuit shown in Fig. 25.32, find (i) input impedance (ii) differential voltage gain.*

Solution.

(i) $$\text{Tail current, } I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{(12 - 0.7)V}{100\ k\Omega} = 113\ \mu A$$

The d.c. emitter current in each transistor is

$$I_{E1} = I_{E2} = I_E/2 = 113\ \mu A/2 = 56.5\ \mu A$$

$$\therefore \quad \text{a.c. emitter resistance, } r_e' = \frac{25\ mV}{I_{E1} \text{ or } I_{E2}} = \frac{25\ mV}{56.5\ \mu A} = 442\ \Omega$$

$\therefore$ Input impedance, $Z_i = 2\beta r'_e = 2 \times 220 \times 442\ \Omega$

$= 194 \times 10^3\ \Omega = \mathbf{194\ k\Omega}$

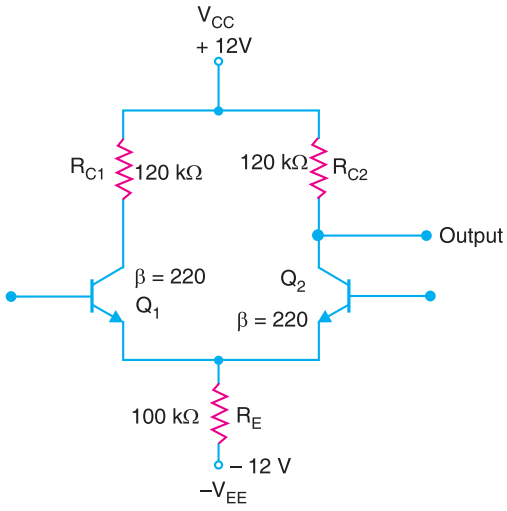


Fig. 25.32

(ii) Differential voltage gain, $A_{DM} = \dfrac{R_{C1} \text{ or } R_{C2}}{2r'_e} = \dfrac{120\ \text{k}\Omega}{2 \times 442\ \Omega} = \mathbf{136}$

Example 25.16. *For the circuit shown in Fig. 25.33, find the differential-mode voltage gain.*

Solution. Because we are taking the output from Q_2, there is no need for collector resistor on Q_1. To find the relevant bias currents, we set the input sources to 0V, connecting the two bases to ground.

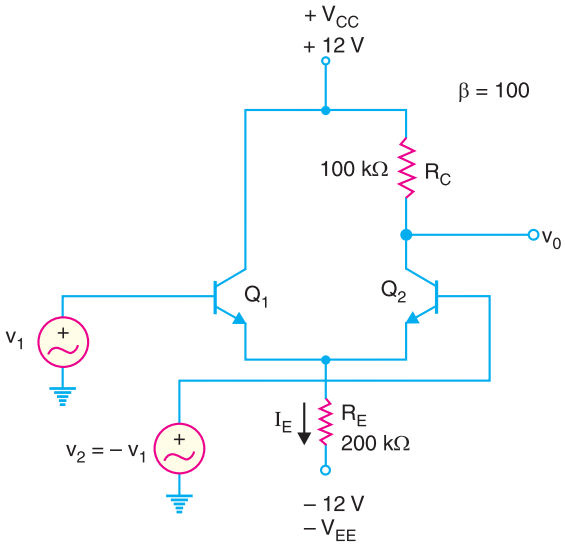


Fig. 25.33

Tail current, $I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{(12 - 0.7)V}{200\ \text{k}\Omega} = 0.0565\ \text{mA}$

Therefore, emitter current in each transistor is

$I_{E1} = I_{E2} = I_E/2 = 0.0565\ \text{mA}/2 = 0.0283\ \text{mA}$

$\therefore$ a.c. emitter resistance, $r'_e = \dfrac{25\text{ mV}}{I_{E1}} = \dfrac{25\text{ mV}}{0.0283\text{ mA}} = 883.4\,\Omega$

$\therefore$ Differential voltage gain, $A_{DM} = \dfrac{R_C}{2r'_e} = \dfrac{100\text{ k}\Omega}{2 \times 883.4\,\Omega} = \mathbf{56.6}$

25.14 Common-mode Voltage Gain (A_{CM})

The common-mode signals are equal in amplitude and have the same phase. Fig. 25.34(*i*) shows the common-mode operation of a differential amplifier (*DA*). Note that the same input voltage, $v_{in(CM)}$ is being applied to each base. Ideally, there is no a.c. output voltage with a common-mode input signal. It is because a differential amplifier is designed to respond to *the difference between two input signals.* If there is no difference between the inputs, the output of *DA* is zero. In practice, the two halves of the differential amplifier are never completely balanced and there is a very small a.c. output voltage for the common-mode signal.

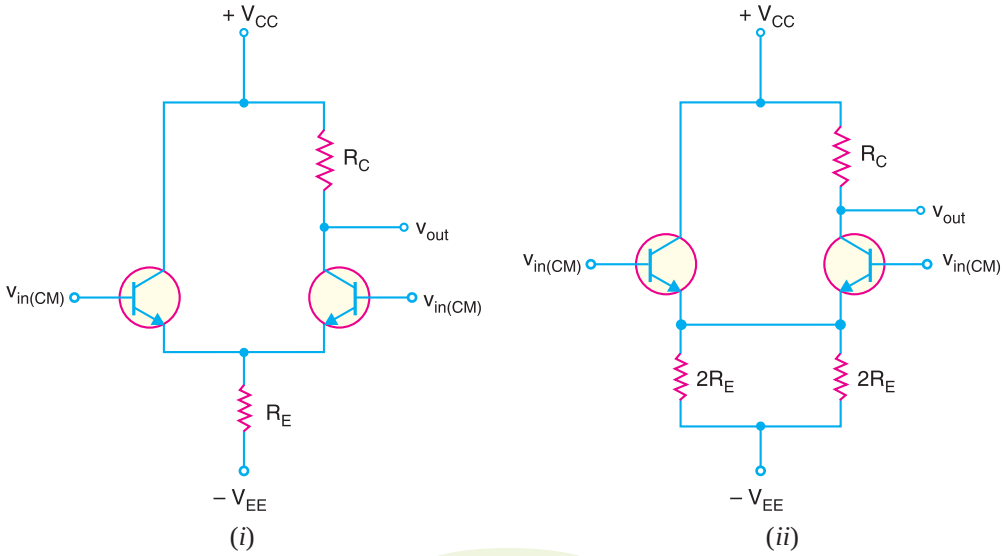


Fig. 25.34

The circuit shown in Fig. 25.34(*i*) can be redrawn as shown in Fig. 25.34(*ii*). In this equivalent circuit, the two parallel resistances of 2 R_E produce an equivalent resistance of R_E. Therefore, this equivalent circuit will not affect the output voltage. Assuming identical transistors, the two emitter currents will be equal and produce the same voltage across emitter resistors. Therefore, there is no current through the wire between the emitters. We can remove this wire and the circuit becomes as shown in Fig. 25.35 (*i*).

A.C. equivalent circuit. To get the a.c. equivalent circuit, we can reduce both supply voltages to zero *i.e.*, we ground each supply point. Replacing the transistors by their a.c. equivalent circuits, we get a.c. equivalent circuit of differential amplifier for commom-mode operation as shown in Fig. 25.35 (*ii*). We can derive the voltage gain of an *unbypassed *CE* circuit. Here we will use 2 R_E in place of R_E.

$\therefore$ Common-mode voltage gain, $A_{CM} = \dfrac{v_{out}}{v_{in(CM)}} = \dfrac{R_C}{r'_e + 2R_E}$

* We have derived the voltage gain of bypassed capacitor *CE* amplifier in Art. 10.13 as : $A_v = R_C / r'_e$. Without bypass capacitor, the emitter is no longer at a.c. ground. Instead, R_E is seen by the a.c. signal between the emitter and ground and effectively adds to r'_e in the above formula. Therefore, voltage gain without the bypass capacitor becomes: $A_v = \dfrac{R_C}{r'_e + R_E}$

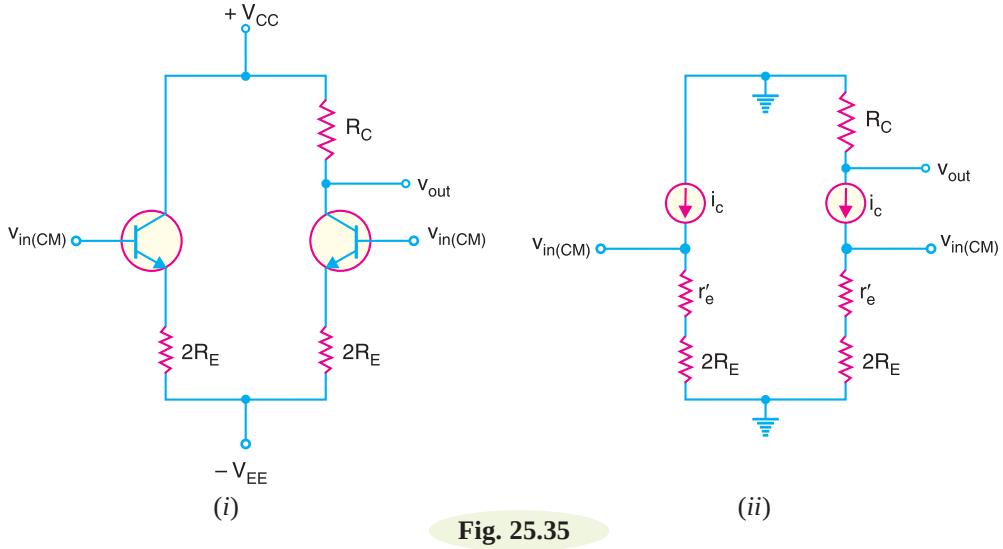


Fig. 25.35

where r'_e = a.c. emitter resistance = $\dfrac{25 \text{ mV}}{\text{d.c. emitter current}}$

In most cases, r'_e is very small as compared to R_E, it (r'_e) is dropped from the formula.

$$\therefore \quad A_{CM} = \frac{R_C}{2R_E}$$

The common-mode voltage gain (A_{CM}) is very small. For example, a typical *DA* may have $R_C = 150$ kΩ and $R_E = 143$ kΩ.

$$\therefore \quad A_{CM} = \frac{R_C}{2R_E} = \frac{150 \text{ k}\Omega}{2 \times 143 \text{ k}\Omega} = 0.52$$

Example 25.17. *Calculate the CMRR for the circuit measurements shown in Fig. 25.36.*

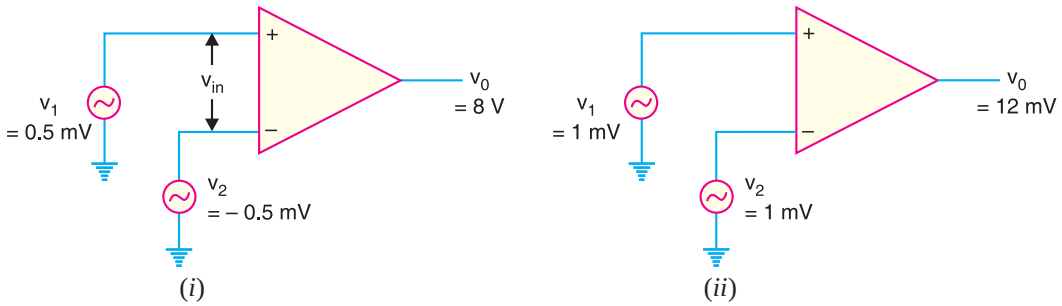


Fig. 25.36

Solution. Fig. 25.36(*i*) shows the differential-mode operation whereas Fig. 25.36(*ii*) shows the common-mode operation. Referring to Fig. 25.36(*i*), $v_{in} = 0.5 - (-0.5) = 1$mV.

$$\therefore \quad \text{Differential voltage gain, } A_{DM} = \frac{v_o}{v_{in}} = \frac{8\text{V}}{1\text{ mV}} = 8000$$

Referring to Fig. 25.36(*ii*), $*v_{in(CM)} = 1$mV

$$\therefore \quad \text{Commom-mode voltage gain, } A_{CM} = \frac{12\text{ mV}}{1\text{ mV}} = 12$$

* Since the output voltage is 12mV, the common-mode signals are not exactly equal in magnitude.

$$\therefore \quad CMRR = \frac{A_{DM}}{A_{CM}} = \frac{8000}{12} = \mathbf{666.7}$$

We can express *CMRR* in dB.

$$CMRR_{dB} = 20\log_{10} CMRR = 20 \log_{10} 666.7 = \mathbf{56.48\ dB}$$

Example 25.18. *The data sheet of an OP-amp gives these typical values : A_{DM} = 200,000 and CMRR = 90 dB. What is the common-mode voltage gain?*

Solution. $90\ dB = 20 \log_{10} CMRR$

$$\therefore \quad CMRR = \text{antilog}\ \frac{90\ dB}{20} = 31,623$$

$$\therefore \quad A_{CM} = \frac{A_{DM}}{CMRR} = \frac{200,000}{31,623} = \mathbf{6.32}$$

Example 25.19. *A differential amplifier has an open-circuit voltage gain of 100. This amplifier has a common input signal of 3.2 V to both terminals. This results in an output signal of 26 mV. Determine (i) common-mode voltage gain (ii) the CMRR in dB.*

Solution.

(*i*) $v_{in(CM)} = 3.2\ V\ ;\ v_{out} = 26\ mV = 26 \times 10^{-3}\ V$

$\therefore$ Common-mode voltage gain, $A_{CM} = \frac{v_{out}}{v_{in(CM)}} = \frac{26 \times 10^{-3}}{3.2} = \mathbf{0.0081}$

(*ii*) $CMRR_{dB} = 20\log_{10} \frac{A_{DM}}{A_{CM}} = 20\log_{10} \frac{100}{0.0081} = \mathbf{81.8\ dB}$

Example 25.20. *For the circuit shown in Fig. 25.37, find (i) the common-mode voltage gain (ii) the CMRR in dB.*

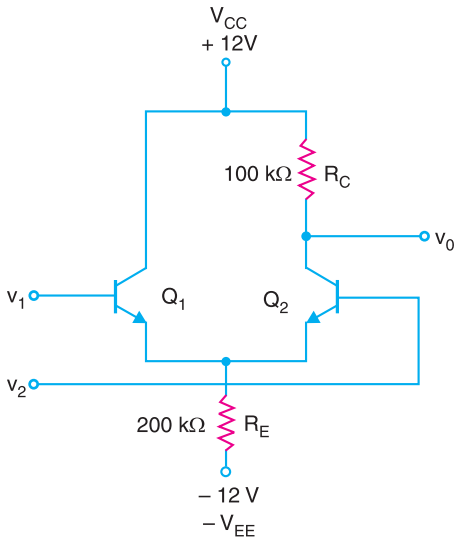


Fig. 25.37

Solution. (*i*) Common-mode voltage gain, $A_{CM} = \frac{R_C}{2R_E} = \frac{100\ k\Omega}{2 \times 200 k\Omega} = \mathbf{0.25}$

(*ii*) In order to find differential voltage gain, we should first find d.c. emitter current.

$$\text{Tail current, } I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{(12 - 0.7)V}{200\ \text{k}\Omega} = 0.0565\ \text{mA}$$

The d.c. emitter current in each transistor is

$$I_{E1} = I_{E2} = I_E/2 = 0.0565\ \text{mA}/2 = 0.0283\ \text{mA}$$

$$\therefore \quad \text{a.c. emitter resistance, } r'_e = \frac{25\ \text{mV}}{I_{E1}} = \frac{25\ \text{mV}}{0.0283} = 883.4\ \Omega$$

$$\therefore \quad \text{Differential voltage gain, } A_{DM} = \frac{R_C}{2r'_e} = \frac{100\ \text{k}\Omega}{2 \times 883.4\ \Omega} = 56.6$$

$$\therefore \quad CMRR_{dB} = 20 \log_{10} \frac{A_{DM}}{A_{CM}} = 20 \log_{10} \frac{56.6}{0.25} = \mathbf{47.09\ dB}$$

25.15 Operational Amplifier (OP- Amp)

Fig. 25.38 shows the block diagram of an operational amplifier (*OP*-amp). The input stage of an *OP*- amp is a differential stage followed by more stages of gain and a class *B* push-pull emitter follower.

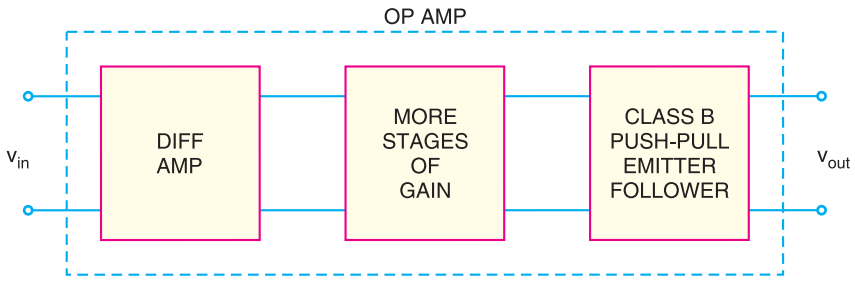


Fig. 25.38

The following are the important properties common to all operational amplifiers (*OP*-amps):

(*i*) An operational amplifier is a multistage amplifier. The input stage of an *OP*-amp is a differential amplifier stage.

(*ii*) An inverting input and a noninverting input.

(*iii*) A high input impedance (usually assumed infinite) at both inputs.

(*iv*) A low output impedance (< 200 Ω).

(*v*) A large open-loop voltage gain, typically 10^5.

(*vi*) The voltage gain remains constant over a wide frequency range.

(*vii*) Very large *CMRR* (> 90 dB).

25.16 Schematic Symbol of Operational Amplifier

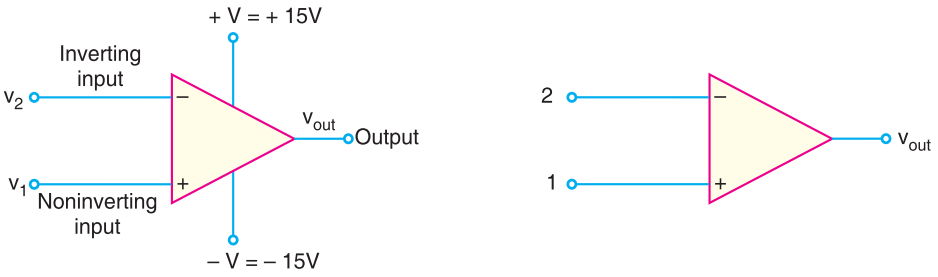
Fig.25.39(*i*) shows the schematic symbol of an operational amplifier. The following points are worth noting :

(*i*) The basic operational amplifier has *five terminals: two terminals for supply voltages +V and –V; two input terminals (inverting input and noninverting input) and one output terminal.

* Two other terminals, the *offset null terminals*, are used to ensure zero output when the two inputs are equal. These are normally used when small d.c. signals are involved.

(*ii*) Note that the input terminals are marked + and –. These are not polarity signs. The – sign indicates the *inverting input* while the + sign indicates the *noninverting input.* A signal applied to plus terminal will appear in the same phase at the output as at the input. A signal applied to the minus terminal will be shifted in phase 180° at the output.

(*iii*) The voltages v_1, v_2 and v_{out} are node voltages. This means that they are always measured w.r.t. ground. The differential input v_{in} is the difference of two node voltages v_1 and v_2. We normally do not show the ground in the symbol.



(*i*) (*ii*)

Fig. 25.39

(*iv*) For the sake of *simplicity, + *V* and – *V* terminals are often omitted from the symbol as shown in Fig. 25.39(*ii*). The two input leads are always shown on the symbol regardless of whether they are both used.

(*v*) In most cases, if only one input is required for an *OP*-amp circuit, the input not in use will be shown connected to ground. A single-input *OP*-amp is generally classified as either inverting or noninverting.

(*vi*) The *OP*-amp is produced as an integrated circuit (*IC*). Because of the complexity of the internal circuitry of an *OP*-amp, the *OP*-amp symbol is used exclusively in circuit diagrams.

25.17 Output Voltage From OP-Amp

The output voltage from an *OP*-amp for a given pair of input voltages depends mainly on the following factors:

1. The voltage gain of *OP*-amp.
2. The polarity relationship between v_1 and v_2.
3. The values of supply voltages, $+V$ and $-V$.

1. Voltage gain of OP-amp. The *maximum* possible voltage gain from a given OP-amp is called *open-loop voltage gain* and is denoted by the symbol A_{OL}. The value of A_{OL} for an *OP*-amp is generally greater than 10,000.

The term open-loop indicates a circuit condition where there is *no feedback path from the output to the input of OP-amp.* The *OP*-amps are almost always operated with negative feedback *i.e.*, a part of the output signal is fed back in phase opposition to the input. Such a condition is

* Since two or more *OP*-amps are often contained in a single *IC* package, eliminating these terminals on the symbol eliminates unnecessary duplication.

illustrated in Fig. 25.40. Here R_i is the input resistance and R_f is the feedback resistor. Consequently, the voltage gain of *OP* amplifier is reduced. When a feedback path is present such as R_f connection in Fig. 25.40, the resulting circuit gain is referred to as *closed-loop voltage gain* (A_{CL}). The following points may be noted :

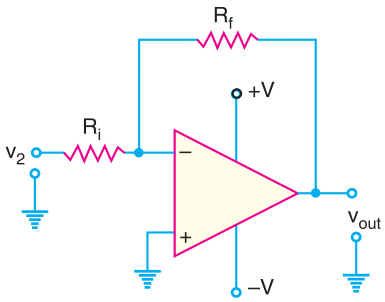


Fig. 25.40

(*i*) The maximum voltage gain of given OP-amp is A_{OL}. Its value is generally greater than 10,000.

(*ii*) The actual gain (A_{CL}) of an OP-amplifier is reduced when negative feedback path exists between output and input.

2. OP-Amp Input/Output Polarity Relationship. The polarity relationship between v_1 and v_2 will determine whether the *OP*-amp output voltage polarity is positive or negative. There is an easy method for it. We know the differential input voltage v_{in} is the difference between the non-inverting input (v_1) and inverting input (v_2) *i.e.*,

$$v_{in} = v_1 - v_2$$

When the result of this equation is *positive*, the OP-amp output voltage will be *positive*. When the result of this equation is *negative*, the output voltage will be *negative*.

Illustration. Let us illustrate *OP*-Amp input/output polarity relationship with numerical values.

(*i*) In Fig. 25.41(*i*), $v_1 = +4V$ and $v_2 = +2V$ so that $v_{in} = v_1 - v_2 = (+4V) - (+2V) = 2V$. Since v_{in} is *positive*, the *OP*-amp output voltage will be *positive*.

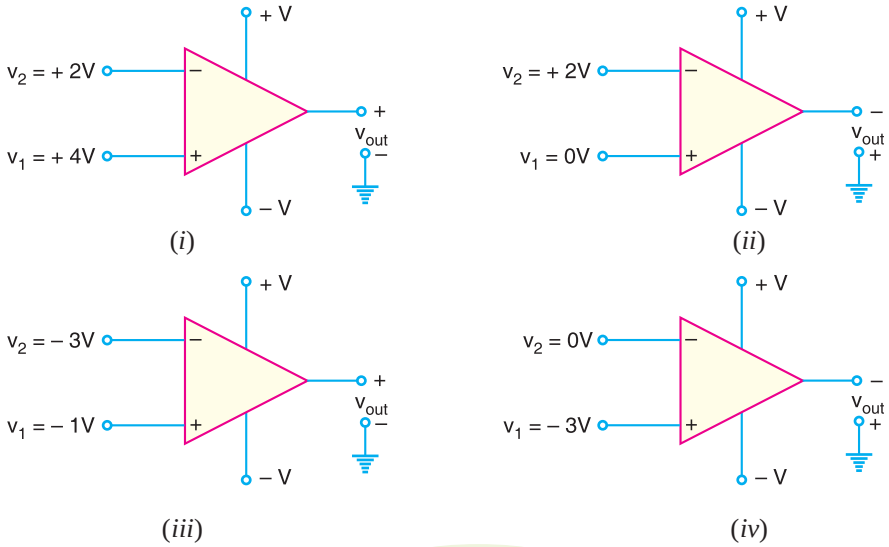


Fig. 25.41

(*ii*) In Fig. 25.41 (*ii*), $v_1 = 0V$ and $v_2 = +2V$ so that $v_{in} = v_1 - v_2 = (0V) - (+2V) = -2V$. Since v_{in} is *negative*, the *OP*-amp output voltage will be *negative*.

(*iii*) In Fig. 25.41 (*iii*), $v_1 = -1V$ and $v_2 = -3V$ so that $v_{in} = v_1 - v_2 = (-1V) - (-3V) = 2V$. Clearly, the *OP*-amp output voltage will be *positive*.

(*iv*) In Fig. 25.41 (*iv*), $v_1 = -3V$ and $v_2 = 0V$ so that $v_{in} = v_1 - v_2 = (-3V) - (0V) = -3V$. Therefore, the *OP*-amp output voltage will be *negative*.

3. Supply Voltages. The supply voltages for an *OP*-amp are normally equal in magnitude and opposite in sign *e.g.*, ± 15V, ± 12V, ± 18*V*. These supply voltages determine the limits of output voltage of *OP*-amp. These limits, known as *saturation voltages,* are generally given by;

$$+V_{sat} = +V_{supply} - 2V$$
$$-V_{sat} = -V_{supply} + 2V$$

Suppose an *OP*-amplifier has $V_{supply} = \pm 15V$ and open-loop voltage gain $A_{OL} = 20{,}000$. Let us find the differential voltage v_{in} to avoid saturation.

$$V_{sat} = V_{supply} - 2 = 15 - 2 = 13V$$

$$\therefore \quad V_{in} = \frac{V_{sat}}{A_{OL}} = \frac{13V}{20,000} = 650\,\mu V$$

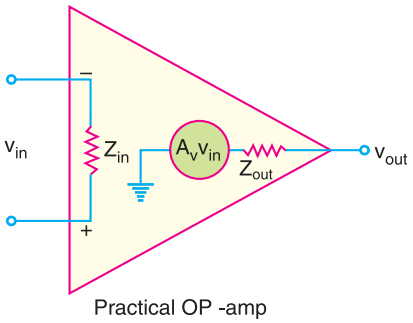
If the differential input voltage V_{in} exceeds this value in an *OP*-amp, it will be driven into saturation and the device will become non-linear.

Note : Although input terminals of an *OP*-amp are labeled as + and –, this does not mean you have to apply positive voltages to the + terminal and negative voltages to the –terminal. Any voltages can be applied to either terminal. The true meaning of the input terminal labels (+ and –) is that a *positive voltage applied to the + terminal drives the output voltage towards +V of d.c. supply; a positive voltage applied to the – terminal drives the output voltage towards –V of d.c. supply.

25.18 A.C. Analysis of OP-Amp

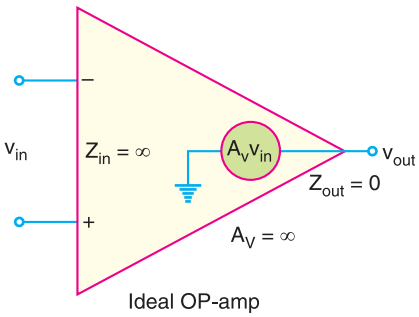
The basic *OP*-amp has two input terminals and one output terminal. The input terminals are labeled as + (noninverting input) and –(inverting input). As discussed earlier, a signal applied to the non-inverting input (+) will produce an output voltage that is in phase with the input voltage. However, a signal applied to the inverting input (–) will produce an output voltage that is 180° out of phase with the input signal.

***(i)* Practical OP–amp.** Fig. 25.42 shows the a.c. equivalent circuit of a practical *OP*-amp. The characteristics of a practical OP-amp are : *very high voltage gain, very high input impedance* and *very low output impedance.* The input voltage v_{in} appears between the two input terminals and the output voltage is $A_v v_{in}$ taken through the output impedance Z_{out}. The consequences of these properties of a practical OP–amp are :



Practical OP -amp

Fig. 25.42



Ideal OP-amp

Fig. 25.43

* Note that positive and negative are relative terms. Thus if +4V is applied at +input terminal and +2V at – input terminal, then + terminal is at more positive potential. Therefore, the output voltage will swing towards +V of d.c. supply.

(*a*) Since the voltage gain (A_v) of a practical *OP*-amp is very high, an extremely small input voltage (v_{in}) will produce a large output voltage (v_{out}).

(*b*) Since the input impedance (Z_{in}) is very high, a practical OP-amp has very small input current.

(*c*) Since the output impedance (Z_{out}) of a practical OP-amp is very low, it means that output voltage is practically independent of the value of load connected to OP-amp.

(*ii*) Ideal OP-amp. Fig. 25.43 shows the a.c. equivalent circuit of an ideal OP-amp. The characteristics of an ideal OP-amp are : *infinite voltage gain, infinite input impedance* and *zero output impedance*. The consequences of these properties of an ideal *OP*-amp are :

(*a*) Since the voltage gain (A_v) of an ideal *OP*-amp is infinite, it means that we can set $v_{in} = 0V$.

(*b*) Since the input impedance (Z_{in}) is infinite, an ideal *OP*-amp has zero input current.

(*c*) Since the output impedance (Z_{out}) of an ideal *OP*-amp is zero, it means the output voltage does not depend on the value of load connected to *OP*-amp.

We can sum up the values of parameters of a practical *OP*-amp and an ideal *OP*-amp as under :

Practical *OP*-amp	**Ideal *OP*-amp**
$Z_{in} = 2\ \text{M}\Omega$	$Z_{in} \to \infty$ (Open circuit)
$A_v = 1 \times 10^5$	$A_v \to \infty$
$Z_{out} = 100\ \Omega$	$Z_{out} = 0\Omega$

25.19 Bandwidth of an OP-Amp

All electronic devices work only over a limited range of frequencies. This range of frequencies is called **bandwidth.** Every *OP*-amp has a bandwidth *i.e.*, the range of frequencies over which it will work properly. The bandwidth of an *OP*-amp depends upon the closed-loop gain of the *OP*-amp circuit. One important parameter is **gain-bandwidth product (GBW).** It is defined as under :

$$A_{CL} \times f_2 = f_{unity} = \text{GBW}$$

where A_{CL} = closed-loop gain at frequency f_2

f_{unity} = frequency at which the closed-loop gain is unity

It can be proved that the gain-bandwidth product of an OP-amp is constant. Since an *OP*-amp is capable of operating as a d.c. amplifier, its bandwidth is ($f_2 - 0$). The gain-bandwidth product of an OP-amp is an important parameter because it can be used to find :

(*i*) The maximum value of A_{CL} at a given value of f_2.

(*ii*) The value of f_2 for a given value of A_{CL}.

Example 25.21. *An OP-amp has a gain-bandwidth product of 15 MHz. Determine the bandwidth of OP-amp when $A_{CL} = 500$. Also find the maximum value of A_{CL} when $f_2 = 200$ kHz.*

Solution.
$$f_2 = \frac{f_{unity}}{A_{CL}} = \frac{15\text{MHz}}{500} = 30\ \text{kHz}$$

Since the *OP*-amp is capable of operating as a d.c. amplifier, bandwidth *BW* = **30 kHz.**

$$A_{CL} = \frac{f_{unity}}{f_2} = \frac{15\text{MHz}}{200\ \text{kHz}} = \textbf{75 or 37.5 db}$$

Example 25.22. *An OP-amp has a gain-bandwidth product of 1.5 MHz. Find the operating bandwidth for the following closed-loop gains* (*i*) $A_{CL} = 1$ (*ii*) $A_{CL} = 10$ (*iii*) $A_{CL} = 100$.

Solution. Bandwidth, $BW = \dfrac{GBW}{A_{CL}}$

(*i*) For $A_{CL} = 1$, $BW = \dfrac{1.5\text{ MHz}}{1} = \mathbf{1.5\text{ MHz}}$

(*ii*) For $A_{CL} = 10$, $BW = \dfrac{1.5\text{ MHz}}{10} = \mathbf{150\text{ kHz}}$

(*iii*) For $A_{CL} = 100$, $BW = \dfrac{1.5\text{ MHz}}{100} = \mathbf{15\text{ kHz}}$

From this example, we conclude that :

(*a*) The higher the gain (A_{CL}) of an *OP*-amp, the narrower its bandwidth.

(*b*) The lower the gain of an *OP*-amp, the wider its bandwidth.

25.20 Slew Rate

The slew rate of an *OP*-amp is a measure of *how fast the output voltage can change* and is measured in volts per microsecond (V/μs). If the slew rate of an *OP*-amp is 0.5V/μs, it means that the output from the amplifier can change by 0.5 V every μs. Since frequency is a function of time, the *slew rate can be used to determine the maximum operating frequency of the OP-amp* as follows:

$$\text{Maximum operating frequency, } f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}}$$

Here V_{pk} is the peak output voltage.

Example 25.23. *Determine the maximum operating frequency for the circuit shown in Fig. 25.44. The slew rate is 0.5 V/μs.*

Solution. The maximum peak output voltage(V_{pk}) is approximately *8*V*. Therefore, maximum operating frequency (f_{max}) is given by;

$$f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}} = \frac{0.5\,V/\mu s}{2\pi \times 8}$$

$$= \frac{500\text{ kHz}}{2\pi \times 8} \quad (\because 0.5\text{ V/μs} = 500\text{ kHz})$$

$$= \mathbf{9.95\text{ kHz}}$$

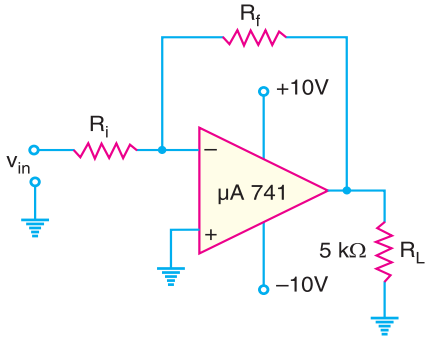


Fig. 25.44

While 9.95 kHz may not seem to be a very high output frequency, you must realise that the amplifier was assumed to be operating at its maximum output voltage. Let us see what happens when peak output voltage is reduced (See example 25.24).

Example 25.24. *The amplifier in Fig. 25.44 is being used to amplify an input signal to a peak output voltage of 100 mV. What is the maximum operating frequency of the amplifier?*

Solution. The maximum operating frequency (f_{max}) of the amplifier is given by;

$$f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}} = \frac{0.5\,V/\mu s}{2\pi \times 0.1} \quad (\because 100\text{ mV} = 0.1\text{V})$$

$$= \frac{500\text{ kHz}}{2\pi \times 0.1} = \mathbf{796\text{ kHz}} \quad (\because 0.5\text{V/μs} = 500\text{ kHz})$$

The above examples show that an *OP*-amp can be operated at a much higher frequency when being used as a small-signal amplifier than when being used as a large-signal amplifier.

* $+V_{sat} = +V_{supply} - 2 = 10 - 2 = 8V$

25.21 Frequency Response of an OP-Amp

The operating frequency has a significant effect on the operation of an *OP*-amp. The following are the important points regarding the frequency response of an *OP*-amp :

(*i*) The maximum operating frequency of an *OP*-amp is given by;

$$f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}}$$

Thus, the *peak output voltage limits the maximum operating frequency.*

(*ii*) When the maximum operating frequency of an *OP*-amp is exceeded, the result is a distorted output waveform.

(*iii*) Increasing the operating frequency of an *OP*-amp beyond a certain point will :

(*a*) Decrease the maximum output voltage swing.

(*b*) Decrease the open-loop voltage gain.

(*c*) Decrease the input impedance.

(*d*) Increase the output impedance.

25.22 OP-Amp with Negative Feedback

An *OP*-amp is almost always operated with negative feedback *i.e.*, a part of the output is fed back in phase opposition to the input (See Fig. 25.45). The reason is simple. The open-loop voltage gain of an *OP*-amp is very high (usually greater than 100,000). Therefore, an extremely small input voltage drives the *OP*-amp into its saturated output stage. For example, assume v_{in} = 1mV and A_{OL} = 100,000. Then,

$$v_{out} = A_{OL}\, v_{in} = (100{,}000) \times (1 \text{ mV}) = 100 \text{ V}$$

Since the output level of an *OP*-amp can never reach 100 V, it is driven deep into saturation and the device becomes non-linear.

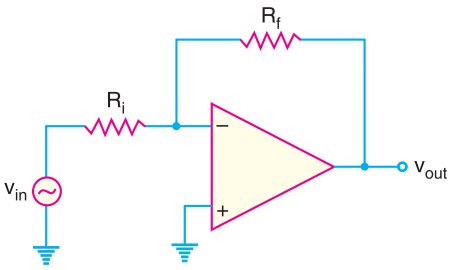


Fig. 25.45

With negative feedback, the voltage gain (A_{CL}) can be reduced and controlled so that OP-amp can function as a linear amplifier. In addition to providing a controlled and stable gain, negative feedback also provides for control of the input and output impedances and amplifier bandwidth. The table below shows the general effects of negative feedback on the performance of OP-amps.

	Voltage gain	Input Z	Output Z	Bandwidth
Without negative feedback	A_{OL} is too high for linear amplifier applications	Relatively high	Relatively low	Relatively narrow
With negative feedback	A_{CL} is set by the feedback circuit to desired value	Can be increased or reduced to a desired value depending on type of circuit	Can be reduced to a desired value	Significantly wider

25.23 Applications of OP-Amps

The operational amplifiers have many practical applications. The *OP*-amp can be connected in a large number of circuits to provide various operating characteristics. In the sections to follow, we shall discuss important applications of *OP*-amps.

25.24 Inverting Amplifier

An *OP* amplifier can be operated as an inverting amplifier as shown in Fig. 25.46. An input signal v_{in} is applied through input resistor R_i to the minus input (inverting input). The output is fed back to the same minus input through feedback resistor R_f. The plus input (noninverting input) is grounded. Note that the resistor R_f provides the **negative feedback*. Since the input signal is applied to the inverting input (–), the output will be inverted (*i.e.* 180° out of phase) as compared to the input. Hence the name inverting amplifier.

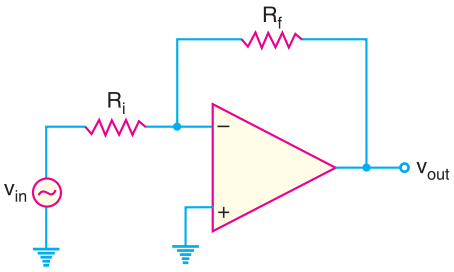
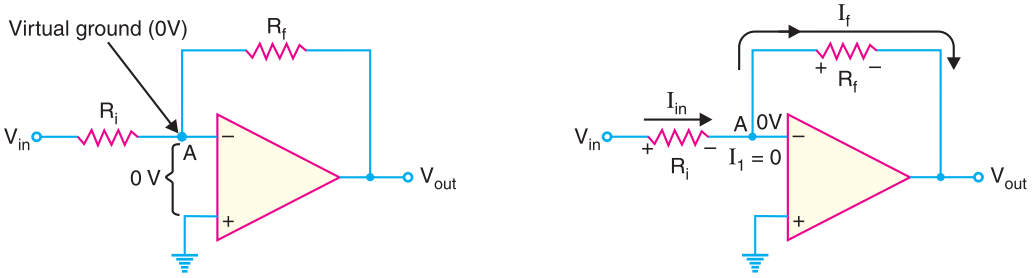


Fig. 25.46

Voltage gain. An OP-amp has an infinite input impedance. This means that there is zero current at the inverting input. If there is zero current through the input impedance, then there must be *no* voltage drop between the inverting and non-inverting inputs. This means that voltage at the inverting input (–) is zero (point *A*) because the other input (+) is grounded. The 0V at the inverting input terminal (point *A*) is referred to as **virtual ground.** This condition is illustrated in Fig. 25.47. The point *A* is said to be at virtual ground because it is at 0V but is not physically connected to the ground (*i.e.* $V_A = 0V$).



(*i*) (*ii*)

Fig. 25.47

Referring to Fig. 25.47 (*ii*), the current I_1 to the inverting input is zero. Therefore, current I_{in} flowing through R_i entirely flows through feedback resistor R_f. In other words, $I_f = I_{in}$.

$$\text{Now} \quad I_{in} = \frac{\text{Voltage across } R_i}{R_i} = \frac{V_{in} - V_A}{R_i} = \frac{V_{in} - 0}{R_i} = \frac{V_{in}}{R_i}$$

$$\text{and} \quad I_f = \frac{\text{Voltage across } R_f}{R_f} = \frac{V_A - V_{out}}{R_f} = \frac{0 - V_{out}}{R_f} = \frac{-V_{out}}{R_f}$$

$$\text{Since } I_f = I_{in}, \quad -\frac{V_{out}}{R_f} = \frac{V_{in}}{R_i}$$

$$\therefore \quad \text{Voltage gain, } A_{CL} = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i}$$

* The output voltage is 180° out of phase with the input. Since the voltage drop across R_f is of the opposite polarity to the applied voltage, the circuit is providing negative feedback.

The negative sign indicates that output signal is inverted as compared to the input signal. The following points may be noted about the inverting amplifier :

(*i*) The closed-loop voltage gain (A_{CL}) of an inverting amplifier is the ratio of the feedback resistance R_f to the input resistance R_i. *The closed-loop voltage gain is independent of the OP-amp's internal open-loop voltage gain.* Thus the negative feedback stabilises the voltage gain.

(*ii*) The inverting amplifier can be designed for unity gain. Thus if $R_f = R_i$, then voltage gain, $A_{CL} = -1$. Therefore, the circuit provides a unity voltage gain with 180° phase inversion.

(*iii*) If R_f is some multiple of R_i, the amplifier gain is constant. For example, if $R_f = 10\ R_i$, then $A_{CL} = -10$ and the circuit provides a voltage gain of exactly 10 along with a 180° phase inversion from the input signal. If we select precise resistor values for R_f and R_i, we can obtain a wide range of voltage gains. *Thus the inverting amplifier provides constant voltage gain.*

25.25 Input and Output Impedance of Inverting Amplifier

It is worthwhile to give a brief discussion about the input impedance and output impedance of inverting amplifier.

(*i*) Input impedance. While an *OP*-amp has an extremely high input impedance, the inverting amplifier does not. The reason for this can be seen by referring back to Fig. 25.47(*i*). As this figure shows, the voltage source "sees" an input resistance (R_i) that is going to virtual ground. Thus the input impedance for the inverting amplifier is

$$Z_i \simeq R_i$$

The value of R_i will always be much less than the input impedance of the *OP*-amp. Therefore, the overall input impedance of an inverting amplifier will also be much lower than the *OP*-amp input impedance.

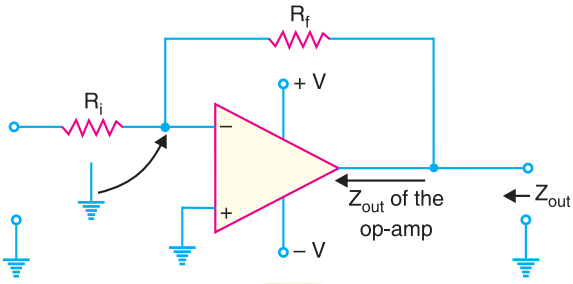


Fig. 25.48

(*ii*) Output impedance. Fig. 25.48 shows the inverting amplifier circuit. You can see from this figure that the output impedance of the inverting amplifier is the parallel combination of R_f and the output impedance of *OP*-amp itself.

The presence of the negative feedback circuit reduces the output impedance of the amplifier to a value that is less than the output impedance of *OP*-amp.

Example 25.25. *Given the OP-amp configuration in Fig. 25.49, determine the value of R_f required to produce a closed-loop voltage gain of –100.*

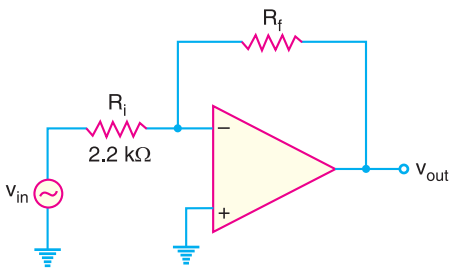


Fig. 25.49

Solution. $A_{CL} = -\frac{R_f}{R_i}$ or $-100 = -\frac{R_f}{2.2}$

$\therefore$ $R_f = 100 \times 2.2 = \mathbf{220\ k\Omega}$

Example 25.26. *Determine the output voltage for the circuit of Fig. 25.50.*

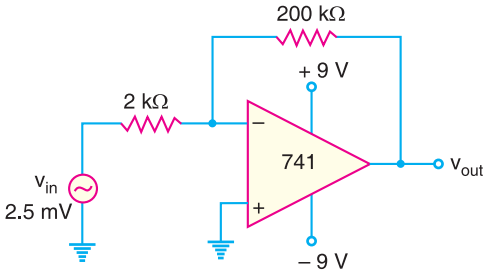


Fig. 25.50

Solution. $A_{CL} = -\frac{R_f}{R_i} = -\frac{200\ k\Omega}{2\ k\Omega} = -100$

$\therefore$ Output voltage, $v_{out} = A_{CL} \times v_{in} = (-100) \times (2.5\ mV) = -250\ mV = \mathbf{-0.25\ V}$

Example 25.27. *Find the output voltage for the circuit shown in Fig. 25.51.*

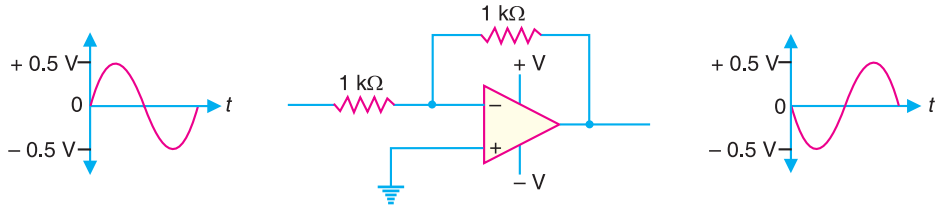


Fig. 25.51

Solution. Voltage gain, $A_{CL} = -\frac{R_f}{R_i} = -\frac{1\ k\Omega}{1\ k\Omega} = -1$

Since the voltage gain of the circuit is –1, the **output will have the same amplitude but with 180° phase inversion.**

Example 25.28. *Find the output voltage for the circuit shown in Fig. 25.52.*

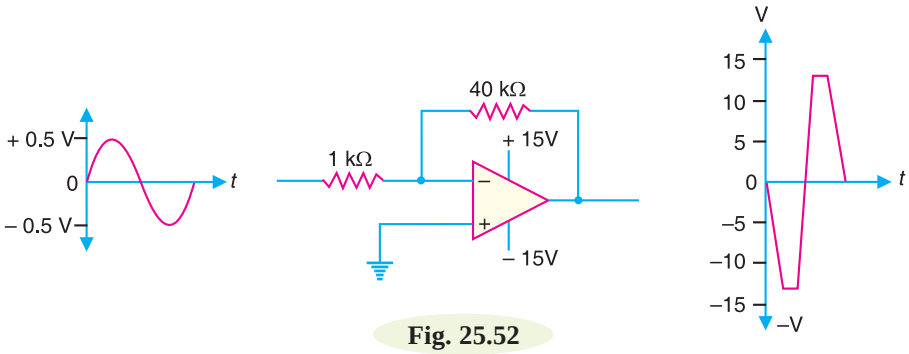


Fig. 25.52

Solution. Voltage gain, $A_{CL} = -\frac{R_f}{R_i} = -\frac{40\ k\Omega}{1\ k\Omega} = -40$

Note that the input signal is the same as in example 25.27 but now the voltage gain is –40 instead of –1. Since the supply voltages are ± 15 V, the *saturation occurs at ± 13 V. Since the output voltage far exceeds the saturation level, the *OP*-amp will be driven to deep saturation and it will behave as a non-linear amplifier. This means that the output will not have the same shape as input but will clip at the saturation voltage. Note that 180° phase inversion does occur.

Example 25.29. *For the circuit shown in Fig. 25.53, find (i) closed-loop voltage gain (ii) input impedance of the circuit (iii) the maximum operating frequency. The slew rate is 0.5V/μs.*

Solution.

(*i*) Closed-loop voltage gain, $A_{CL} = -\frac{R_f}{R_i} = -\frac{100\ \text{k}\Omega}{10\ \text{k}\Omega} = \mathbf{-10}$

(*ii*) The input impedance Z_i of the circuit is

$$Z_i \simeq R_i = \mathbf{10\ k\Omega}$$

(*iii*) To calculate the maximum operating frequency (f_{max}) for this inverting amplifier, we need to determine its peak output voltage. With values of $V_{in} = 1\ V_{pp}$ and $A_{CL} = 10$, the peak-to-peak output voltage is

$$V_{out} = (1V_{pp})\,(A_{CL})$$
$$= (1V_{pp}) \times 10 = 10\ V_{pp}$$

Therefore, the peak output voltage is

$$V_{pk} = 10/2 = 5\ \text{V}$$

$$\therefore \quad f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}} = \frac{0.5\ \text{V}/\mu\text{s}}{2\pi \times 5}$$

$$= \frac{500\ \text{kHz}}{2\pi \times 5} = \mathbf{15.9\ kHz}$$

($\because$ 0.5 V/μs = 500 kHz)

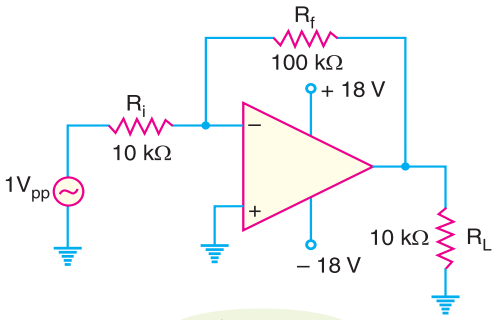


Fig. 25.53

Example 25.30. *You have the following resistor values available:*

1 kΩ; 5 kΩ ; 10 kΩ and 20 kΩ

Design the OP-amp circuit to have a voltage gain of –4.

Solution. Since the voltage gain is negative, the *OP*-amp is operating as an inverting amplifier.

Now, $A_{CL} = -\frac{R_f}{R_i} = -4$

We need to use resistors that have a ratio of 4 : 1. The two resistors which satisfy this requirement are : $R_f = \mathbf{20\ k\Omega}$ and $R_i = \mathbf{5k\Omega.}$

Example 25.31. *Fig. 25.54 shows an inverting OP-amp. Find the closed-loop gain if (i) R_{source} = 0Ω (ii) R_{source} = 1 kΩ.*

Solution. (*i*) When $R_{source} = 0\ \Omega$; $A_{CL} = -\frac{R_f}{R_i} = -\frac{100\ \text{k}\Omega}{1\ \text{k}\Omega} = \mathbf{-100}$

(*ii*) When $R_{source} = 1\ \text{k}\Omega$; $A_{CL} = -\frac{R_f}{R_{source} + R_i} = -\frac{100\ \text{k}\Omega}{1\ \text{k}\Omega + 1\ \text{k}\Omega} = \mathbf{-50}$

Note that we have lost half of the voltage gain.

* $+V_{sat} = +V_{supply} - 2\ \text{V} = +15\ \text{V} - 2\ \text{V} = +13\ \text{V}$
$-V_{sat} = -V_{supply} + 2\ \text{V} = -15\ \text{V} + 2\ \text{V} = -13\ \text{V}$

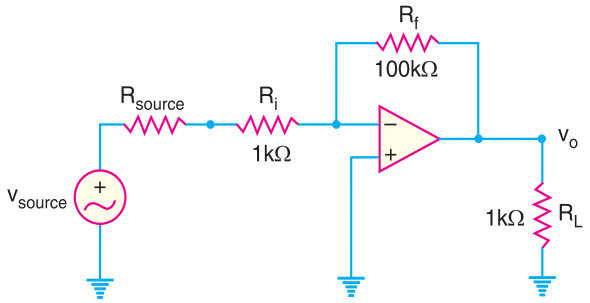


Fig. 25.54

25.26 Noninverting Amplifier

There are times when we wish to have an output signal of the same polarity as the input signal. In this case, the *OP*-amp is connected as noninverting amplifier as shown in Fig. 25.55. The input signal is applied to the noninverting input (+). The output is applied back to the input through the feedback circuit formed by feedback resistor R_f and input resistance R_i. Note that resistors R_f and R_i form a voltage divide at the inverting input (–). This produces **negative feedback* in the circuit. Note that R_i is grounded. Since the input signal is applied to the noninverting input (+), the output signal will be noninverted i.e., the output signal will be in phase with the input signal. Hence, the name non-inverting amplifier.

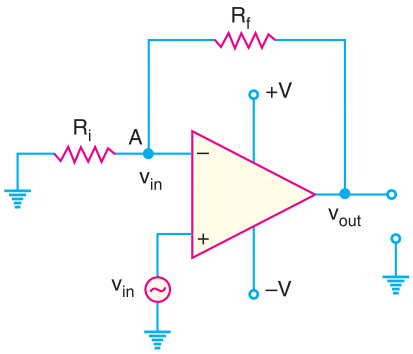


Fig. 25.55

Voltage gain. If we assume that we are not at saturation, the potential at point *A* is the same as V_{in}. Since the input impedance of *OP*-amp is very high, all of the current that flows through R_f also flows through R_i. Keeping these things in mind, we have,

$$\text{Voltage across } R_i = V_{in} - 0 \;;\; \text{Voltage across } R_f = V_{out} - V_{in}$$

Now $\quad$ Current through R_i = Current through R_f

or $$\frac{V_{in} - 0}{R_i} = \frac{V_{out} - V_{in}}{R_f}$$

or $$V_{in} R_f = V_{out} R_i - V_{in} R_i$$

or $$V_{in} (R_f + R_i) = V_{out} R_i$$

or $$\frac{V_{out}}{V_{in}} = \frac{R_f + R_i}{R_i} = 1 + \frac{R_f}{R_i}$$

$\therefore$ Closed-loop voltage gain, $A_{CL} = \dfrac{V_{out}}{V_{in}} = 1 + \dfrac{R_f}{R_i}$

The following points may be noted about the noninverting amplifier :

(*i*) $$A_{CL} = 1 + \frac{R_f}{R_i}$$

* If the output voltage increases, the voltage at the inverting input will also increase. Since the voltage being amplified is the difference between the voltages at the two input terminals, the differential voltage will decrease when the output voltage increases. Therefore, the circuit provides negative feedback.

The voltage gain of noninverting amplifier also depends upon the values of R_f and R_i.

(ii) The voltage gain of a non-inverting amplifier can be made equal to or greater than 1.

(iii) The voltage gain of a non-inverting amplifier will always be greater than the gain of an equivalent inverting amplifier by a value of 1. If an inverting amplifier has a gain of 150, the equivalent noninverting amplifier will have a gain of 151.

(iv) The voltage gain is positive. This is not surprising because output signal is in phase with the input signal.

Non-inverting operational amplifier.

25.27 Voltage Follower

The voltage follower arrangement is a special case of noninverting amplifier where all of the output voltage is fed back to the inverting input as shown in Fig. 25.56. Note that we remove R_i and R_f from the noninverting amplifier and short the output of the amplifier to the inverting input. The voltage gain for the voltage follower is calculated as under :

$$A_{CL} = 1 + \frac{R_f}{R_i} = 1 + \frac{0}{R_i} = 1 \qquad (\because R_f = 0\Omega)$$

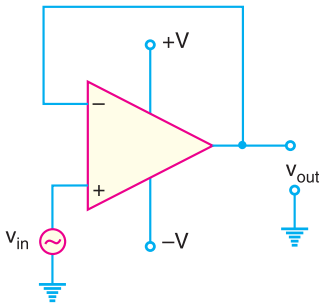


Fig. 25.56

Thus the closed-loop voltage gain of the voltage follower is 1. The most important features of the voltage follower configuration are its *very high input impedance* and its *very low output impedance*. These features make it a nearly ideal buffer amplifier to be connected between high-impedance sources and low-impedance loads.

Example 25.32. *Calculate the output voltage from the noninverting amplifier circuit shown in Fig. 25.57 for an input of 120 μV.*

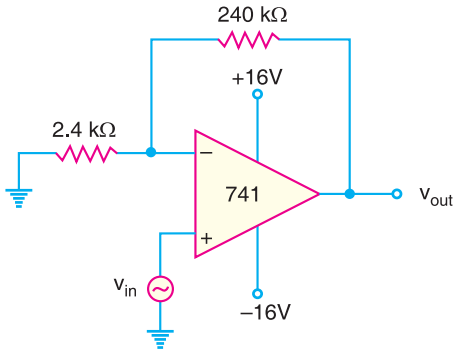


Fig. 25.57

Solution. Voltage gain, $A_{CL} = 1 + \frac{R_f}{R_i} = 1 + \frac{240\ \text{k}\Omega}{2.4\ \text{k}\Omega} = 1 + 100 = 101$

Output voltage, $v_{out} = A_{CL} \times v_{in} = (101) \times (120\ \mu\text{V}) =$ **12.12 mV**

Example 25.33. *For the noninverting amplifier circuit shown in Fig. 25.58, find the output voltage for an input voltage of (i) 1 V (ii) –1 V.*

Solution. Voltage gain, $A_{CL} = 1 + \frac{R_f}{R_i} = 1 + \frac{10\ \text{k}\Omega}{1\ \text{k}\Omega} = 1 + 10 = 11$

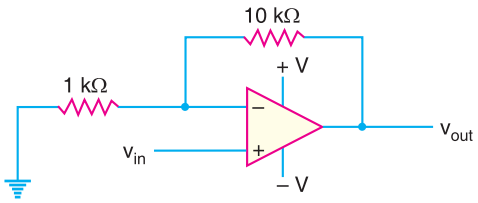


Fig. 25.58

(i) For $v_{in} = 1$ V ; $v_{out} = A_{CL} \times v_{in} = 11 \times 1$ V = **11 V**

(ii) For $v_{in} = -1$ V ; $v_{out} = A_{CL} \times v_{in} = 11 \times (-1$ V$) =$ **– 11 V**

Example 25.34. *For the noninverting amplifier circuit shown in Fig. 25.59, find peak-to-peak output voltage.*

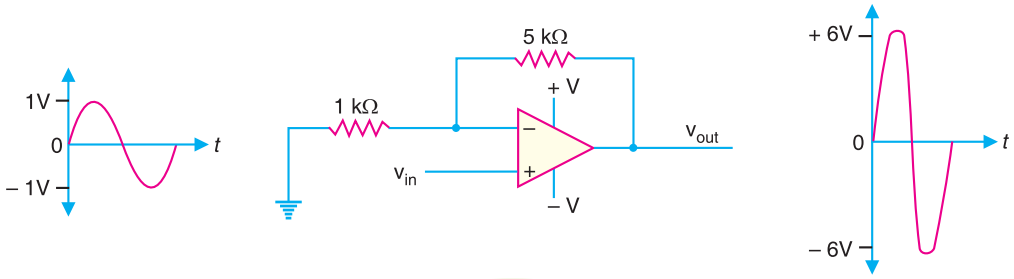


Fig. 25.59

Solution. The input signal is 2 *V* peak-to-peak.

Voltage gain, $A_{CL} = 1 + \frac{R_f}{R_i} = 1 + \frac{5\ \text{k}\Omega}{1\ \text{k}\Omega} = 1 + 5 = 6$

∴ Peak-to-peak output voltage $= A_{CL} \times v_{inpp} = 6 \times 2 =$ **12 V**

Example 25.35. *For the noninverting amplifier circuit shown in Fig. 25.60, find (i) closed-loop voltage gain (ii) maximum operating frequency. The slew rate is 0.5 V/μs.*

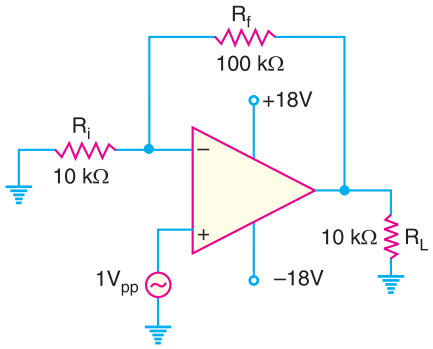


Fig. 25.60

Solution.

(*i*) Voltage gain, $A_{CL} = 1 + \dfrac{R_f}{R_i} = 1 + \dfrac{100\ \text{k}\Omega}{10\ \text{k}\Omega} = 1 + 10 = \mathbf{11}$

(*ii*) To determine the value of maximum operating frequency (f_{max}), we need to calculate the peak output voltage for the amplifier. The peak-to-peak output voltage is

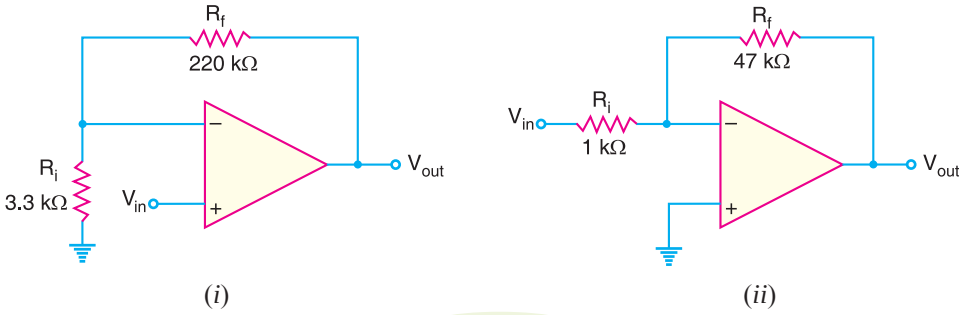
$$v_{out} = A_{CL} \times v_{in} = 11 \times (1V_{pp}) = 11V_{pp}$$

$\therefore$ Peak output voltage, $V_{pk} = 11/2 = 5.5$ V

$\therefore$ $$f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}} = \frac{0.5\ \text{V/}\mu\text{s}}{2\pi \times 5.5}$$

$$= \frac{500\ \text{kHz}}{2\pi \times 5.5} = \mathbf{14.47\ kHz} \qquad (\because\ 0.5\ \text{V/}\mu\text{s} = 500\ \text{kHz})$$

Example 25.36. *Determine the bandwidth of each of the amplifiers in Fig. 25.61. Both OP-amps have an open-loop voltage gain of 100 dB and a unity-gain bandwidth of 3MHz.*



(*i*) (*ii*)

Fig. 25.61

Solution.

(*i*) For the noninverting amplifier shown in Fig. 25.61 (*i*), the closed-loop voltage gain (A_{CL}) is

$$A_{CL} = 1 + \frac{R_f}{R_i} = 1 + \frac{220\ \text{k}\Omega}{3.3\ \text{k}\Omega} = 1 + 66.7 = 67.7$$

$\therefore$ Bandwidth, $BW = \dfrac{\text{Unity-gain } BW}{A_{CL}} = \dfrac{3\ \text{MHz}}{67.7} = \mathbf{44.3\ kHz}$

(*ii*) For the inverting amplifier shown in Fig. 25.61 (*ii*),

$$A_{CL} = -\frac{R_f}{R_i} = -\frac{47\ \text{k}\Omega}{1\ \text{k}\Omega} = -47$$

$\therefore$ Bandwidth, $BW = \dfrac{3\ \text{MHz}}{47} = \mathbf{63.8\ kHz}$

Example 25.37. *Fig. 25.62 shows the circuit of voltage follower. Find* (i) *the closed-loop voltage gain and* (ii) *maximum operating frequency. The slew rate is 0.5 V/μs.*

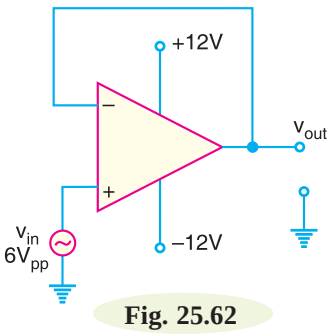


Fig. 25.62

Solution.

(*i*) For the voltage follower, $A_{CL} = \mathbf{1}$

(ii) Since $A_{CL} = 1$ for the circuit, $v_{out} = v_{in}$. Therefore, peak output voltage (V_{pk}) is one-half of $6V_{pp}$ *i.e.*, $V_{pk} = 6/2 = 3$ V. The maximum operating frequency (f_{max}) is given by ;

$$f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}} = \frac{0.5 \text{ V/}\mu\text{s}}{2\pi \times 3}$$

$$= \frac{500 \text{ kHz}}{2\pi \times 3} = \mathbf{26.53\ kHz} \qquad (\because 0.5 \text{ V/}\mu\text{s} = 500 \text{ kHz})$$

25.28 Multi-stage OP-Amp Circuits

When a number of OP-amp stages are connected in series, the overall voltage gain is equal to the product of individual stage gains. Fig. 25.63 shows connection of three stages. The first stage is connected to provide noninverting gain. The next two stages provide inverting gains.

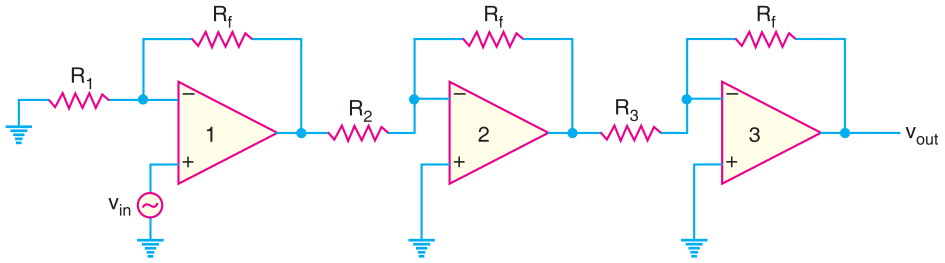


Fig. 25.63

The overall voltage gain A of this circuit is given by;

$$A = A_1A_2A_3$$

where A_1 = Voltage gain of first stage = $1 + (R_f/R_1)$

A_2 = Voltage gain of second stage = $-R_f/R_2$

A_3 = Voltage gain of third stage = $-R_f/R_3$

Since the overall voltage gain is positive, the circuit behaves as a noninverting amplifier.

Example 25.38. *Fig. 25.63 shows the multi-stage OP-amp circuit. The resistor values are : R_f = 470 kΩ ; R_1 = 4.3 kΩ ; R_2 = 33 kΩ and R_3 = 33 kΩ. Find the output voltage for an input of 80 μV.*

Solution. Voltage gain of first stage, $A_1 = 1 + (R_f/R_1) = 1 + (470 \text{ k}\Omega/4.3 \text{ k}\Omega) = 110.3$

Voltage gain of second stage, $A_2 = -R_f/R_2 = -470 \text{ k}\Omega/33 \text{ k}\Omega = -14.2$

Voltage gain of third stage, $A_3 = -R_f/R_3 = -470 \text{ k}\Omega/33 \text{ k}\Omega = -14.2$

$\therefore$ Overall voltage gain, $A = A_1A_2A_3 = (110.3) \times (-14.2) \times (-14.2) = 22.2 \times 10^3$

Output voltage, $v_{out} = A \times v_{in} = 22.2 \times 10^3 \times (80\ \mu\text{V}) = \mathbf{1.78V}$

Example 25.39. *A three-stage OP-amp circuit is required to provide voltage gains of +10, –18 and –27. Design the OP-amp circuit. Use a 270 kΩ feedback resistor for all three circuits. What output voltage will result for an input of 150 μV?*

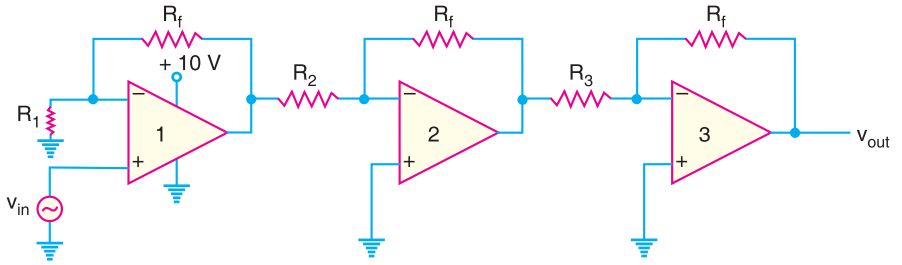


Fig. 25.64

Solution. Designing the above OP-amp circuit means to find the values of R_1, R_2 and R_3. The first stage gain is +10 so that this stage operates as noninverting amplifier.

Now $$+10 = 1 + \frac{R_f}{R_1} \quad \therefore \quad R_1 = \frac{R_f}{10-1} = \frac{270\ \text{k}\Omega}{9} = \mathbf{30\ k\Omega}$$

The second stage gain is –18 so that this stage operates as an inverting amplifier.

$$\therefore \quad -18 = -\frac{R_f}{R_2} \quad \text{or} \quad R_2 = \frac{R_f}{18} = \frac{270\ \text{k}\Omega}{18} = \mathbf{15\ k\Omega}$$

The third stage gain is –27 so that this stage operates as an inverting amplifier.

$$\therefore \quad -27 = -\frac{R_f}{R_3} \quad \text{or} \quad R_3 = \frac{R_f}{27} = \frac{270\ \text{k}\Omega}{27} = \mathbf{10\ k\Omega}$$

Overall voltage gain, $A = A_1A_2A_3 = (10) \times (-18) \times (-27) = 4860$

Output voltage, $v_{out} = A \times v_{in} = (4860) \times (150\ \mu\text{V}) = \mathbf{0.729\ V}$

Example 25.40. *Show the connection of three OP-amp stages using an LM 348 IC to provide outputs that are 10, 20, and 50 times larger than the input and 180° out of phase w.r.t. input. Use a feedback resistor of R_f = 500 kΩ in all stages.*

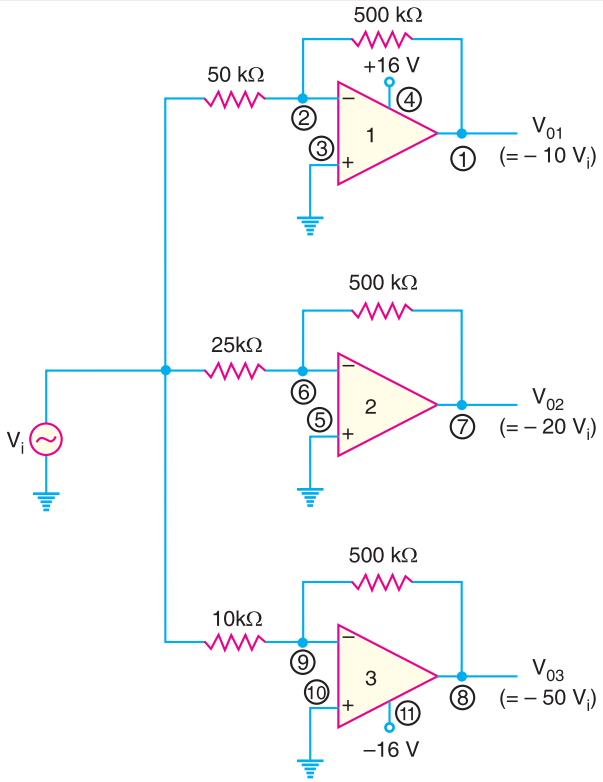


Fig. 25.65

Solution. The resistor component for each stage will be :

$$R_1 = -\frac{R_f}{A_1} = -\frac{500\ \text{k}\Omega}{-10} = \mathbf{50\ k\Omega}$$

$$R_2 = -\frac{R_f}{A_2} = -\frac{500\ \text{k}\Omega}{-20} = \mathbf{25\ k\Omega}$$

$$R_3 = -\frac{R_f}{A_3} = -\frac{500\ \text{k}\Omega}{-50} = \mathbf{10\ k\Omega}$$

The resulting circuit is shown in Fig. 25.65.

25.29 Effect of Negative Feedback on OP-Amp Impedances

In a negative feedback amplifier, a part of the output is fed in phase opposition to the input. The negative feedback produces remarkable changes in the circuit performance. The advantages of negative feedback are : stable gain, less distortion, increased bandwidth and affecting the input impedance and output impedance of the circuit. We now discuss the effect of negative feedback on the impedances of both noninverting and inverting amplifiers.

(*i*) Noninverting Amplifier. (Fig. 25.66). The expressions for the input and output impedances on account of negative voltage feedback in noninverting amplifier are the same as for discrete amplifier (Art. 13.4).

$$Z_{in}\,(*NI) = Z_{in}(1 + m_v A_{OL})$$

$$Z_{out}\,(NI) = \frac{Z_{out}}{1 + m_v A_{OL}}$$

where
Z_{in}, Z_{out} = impedance values without feedback
$Z_{in}(NI)$, $Z_{out}(NI)$ = impedance values with negative feedback
m_v = feedback factor
A_{OL} = voltage gain without feedback = open-loop gain

Note that negative feedback in noninverting amplifier has greatly increased the input impedance and at the same time decreased the output impedance. The increased impedance is an advantage because the amplifier will now present less of a load to its source circuit.

The decreased output impedance is also a benefit because the amplifier will be better suited to drive low impedance loads.

Voltage-follower (*VF*) impedances. Since voltage follower is a special case of noninverting amplifier with feedback fraction $m_v = 1$,

$$\therefore \quad Z_{in(VF)} = Z_{in}\,(1 + A_{OL})$$

$$Z_{out(VF)} = \frac{Z_{out}}{1 + A_{OL}}$$

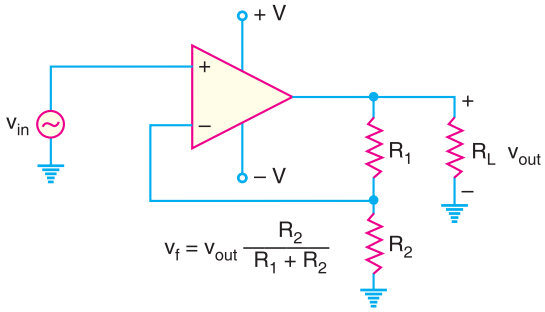


Fig. 25.66

Noninverting feedback amplifier.

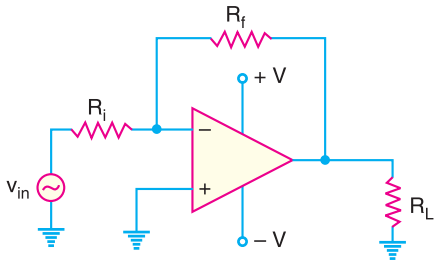


Fig. 25.67

Inverting feedback amplifier.

* Note that '*NI*' means noninverting amplifier.

Note that the voltage-follower input impedance is greater for given Z_{in} and A_{OL} than for the non-inverting configuration with the voltage-divider feedback circuit. Also, its output impedance is much smaller.

(*ii*) Inverting Amplifier. Fig. 25.67 shows the inverting amplifier. It can be shown that :

Input impedance, $Z_{in(*I)} \simeq R_i$

Output impedance, $Z_{out(I)} \simeq Z_{out}$ of *OP*-amp

Note that *the addition of negative voltage feedback to the inverting OP-amp reduces the input impedance of the circuit.* The reduction of Z_{in} is the primary difference betwen the inverting and the noninverting negative feedback circuits. Otherwise, the effects of negative voltage feedback are nearly identical for the two circuits.

Example 25.41. (*i*) *Determine the input and output impedances of the amplifier in Fig. 25.68. The OP-amp date sheet gives* $Z_{in} = 2\ M\Omega$, $Z_{out} = 75\ \Omega$ *and open loop gain of 200,000.*

(*ii*) *Find the closed-loop voltage gain.*

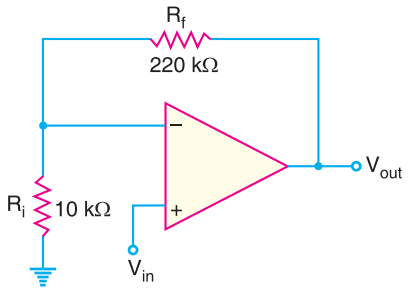


Fig. 25.68

Solution.

(*i*) Feedback fraction, $m_v = \dfrac{R_i}{R_i + R_f} = \dfrac{10\ k\Omega}{10\ k\Omega + 220\ k\Omega} = \dfrac{10\ k\Omega}{230\ k\Omega} = 0.043$

Input impedance, $Z_{in(NI)} = Z_{in}\,(1 + A_{OL}m_v)$

$= (2M\Omega)\ [(1 + 200,\ 000 \times 0.043)]$

$= (2M\Omega)\ [\ 1 + 8600] = \mathbf{17{,}202\ M\Omega}$

Output impedance, $Z_{out(NI)} = \dfrac{Z_{out}}{1 + A_{OL}m_v} = \dfrac{75\ \Omega}{1 + 8600} = \mathbf{8.7 \times 10^{-3}\ \Omega}$

(*ii*) Closed-loop voltage gain, $A_{CL} = 1 + \dfrac{R_f}{R_i} = 1 + \dfrac{220\ k\Omega}{10\ k\Omega} = \mathbf{23}$

Comments. Note the effect of negative voltage feedback on noninverting amplifier.

(*a*) Input and output signals are in phase.

(*b*) A virtually infinite input impedance.

(*c*) Virtually zero output impedance.

Example 25.42. *The same OP-amp in example 25.41 is used in a voltage-follower arrangement. Determine the input and output impedances.*

Solution. For voltage follower, feedback factor $m_v = 1$.

$\therefore \quad Z_{in(VF)} = Z_{in}(1 + A_{OL}) = 2M\Omega\ (1 + 200{,}000) = \mathbf{400{,}002\ M\Omega}$

$Z_{out(VF)} = \dfrac{Z_{out}}{1 + A_{OL}} = \dfrac{75\ \Omega}{1 + 200{,}000} = \mathbf{0.38 \times 10^{-3}\ \Omega}$

* Note that "*I*" means inverting amplifier.

Note that $Z_{in(VF)}$ is much greater than $Z_{in(NI)}$ and $Z_{out(VF)}$ is much less than $Z_{out(NI)}$ from example 25.41.

Example 25.43. *Find the values of the input and output impedances in Fig. 25.69. Also determine the closed-loop voltage gain. The OP-amp has the following parameters: Z_{in} = 4 MΩ; Z_{out} = 50 Ω and open-loop voltage gain = 50,000.*

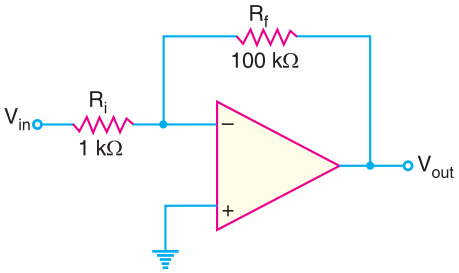


Fig. 25.69

Solution.

$$Z_{in}(I) \simeq R_i = \mathbf{1\ k\Omega}$$

$$Z_{out}(I) \simeq Z_{out} = \mathbf{50\ \Omega}$$

$$A_{CL} = -\frac{R_f}{R_i} = -\frac{100\ k\Omega}{1\ k\Omega} = \mathbf{-100}$$

25.30 Faults in Feedback Circuit

A failure of the feedback circuit in an *OP*-amp is one of the easiest problems in the world to locate. The most noticeable effect is that *voltage gain of the amplifier will change drastically*. Sometimes the gain will increase; sometimes it will decrease. It all depends on which component goes bad. For example, consider the circuit shown in Fig. 25.70.

***(i)* Under normal conditions:** Under normal conditions, the output from the amplifier is $v_{out} = A_{CL}\ v_{in}$. The waveform would be correct. This is shown in Fig. 25.70 (*i*)

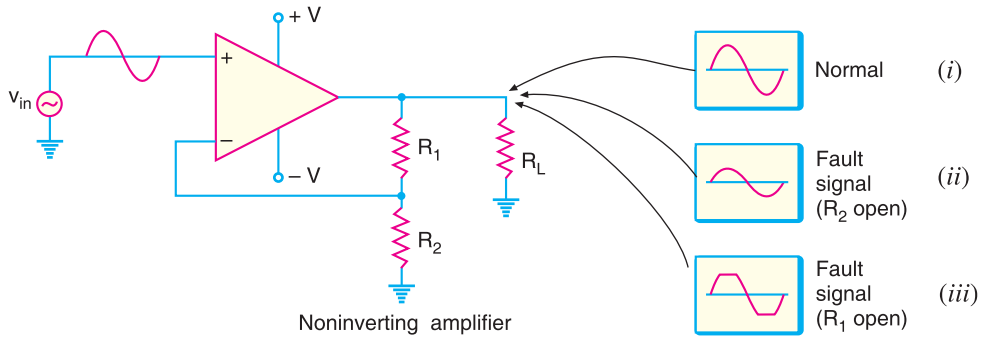


Fig. 25.70

***(ii)* When R_2 is open:** If R_2 opens, the feedback circuit would consist solely of R_1. In this case, the gain would *drop*. It is because the circuit would now act as a *voltage follower. In other words, the circuit would now be a buffer with an output voltage that is equal to the input voltage. Thus we would have the output signal as shown in Fig. 25.70 (*ii*). The waveform would be correct but we would have unity gain.

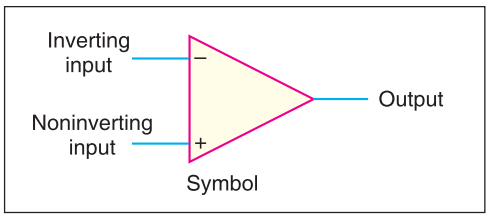
***(iii)* When R_1 is open:** When R_1 opens, the entire feedback circuit would be effectively removed. This would cause the gain of the amplifier to increase to the value of open-loop gain A_{OL}. Clearly, the output voltage will clip at or near the values of +*V* and – *V*. This results in the distorted output signal as shown in Fig. 25.70 (*iii*).

* $A_{CL} = 1 + \frac{R_f}{R_i} = 1 + \frac{R_1}{R_2} = 1 + \frac{R_1}{\infty} = 1 + 0 = 1$

Under these conditions, the closed-loop voltage gain would be unity.

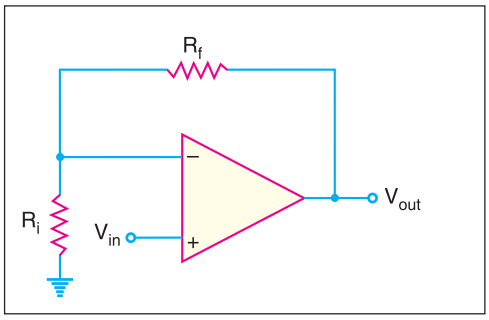
25.31 Summary of OP-AMP Configurations

Basic OP-AMP



- Very high open-loop voltage gain
- Very high input impedance
- Very low output impedance

Noninverting Amplifier



- Voltage gain:

$$A_{CL}(NI) = 1 + \frac{R_f}{R_i}$$

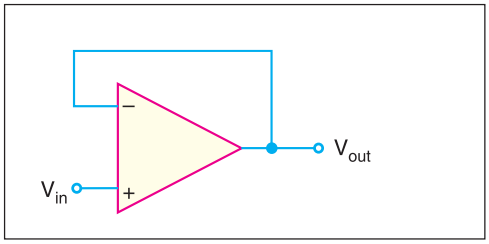
- Input impedance:

$$Z_{in(NI)} = (1 + A_{OL} m_v)\, Z_{in}$$

- Output impedance:

$$Z_{out(NI)} = \frac{Z_{out}}{1 + A_{OL} m_v}$$

Voltage Follower



- Voltage gain:

$$A_{CL(VF)} = 1$$

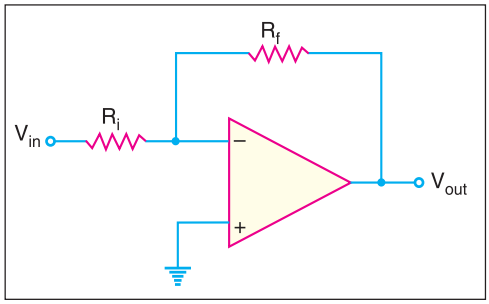
- Input impedance:

$$Z_{in(VF)} = (1 + A_{OL})\, Z_{in}$$

- Output impedance:

$$Z_{out(VF)} = \frac{Z_{out}}{1 + A_{OL}}$$

Inverting Amplifier



- Voltage gain:

$$A_{CL} = -\frac{R_f}{R_i}$$

- Input impedance:

$$Z_{in(I)} \simeq R_i$$

- Output impedance:

$$Z_{out(I)} \simeq Z_{out}$$

25.32 Summing Amplifiers

A summing amplifier is an inverted *OP*-amp that can accept two or more inputs. *The output voltage of a summing amplifier* is *proportional to the negative of the algebraic sum of its input voltages*. Hence the name **summing amplifier**. Fig. 25.71 shows a three-input summing amplifier but any number of inputs can be used. Three voltages V_1, V_2 and V_3 are applied to the inputs and produce

currents I_1, I_2 and I_3. Using the concepts of infinite impedance and virtual ground, you can see that inverting input of the *OP*-amp is at virtual ground ($0V$) and there is no current to the input. This means that the three input currents I_1, I_2 and I_3 combine at the summing point A and form the total current (I_f) which goes through R_f as shown in Fig. 25.71.

$$\therefore \quad I_f = I_1 + I_2 + I_3$$

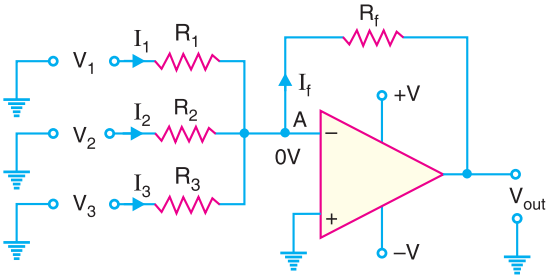


Fig. 25.71

When all the three inputs are applied, the output voltage is

$$\text{Output voltage, } V_{out} = -I_f R_f = -R_f(I_1 + I_2 + I_3)$$

$$= -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$$

$$\therefore \quad V_{out} = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$$

If $R_1 = R_2 = R_3 = R$, then, we have,

$$V_{out} = -\frac{R_f}{R}(V_1 + V_2 + V_3)$$

Thus the output voltage is proportional to the algebraic sum of the input voltages (of course neglecting negative sign). An interesting case results when the **gain of the amplifier is unity.** In that case, $R_f = R_1 = R_2 = R_3$ and output voltage is

$$V_{out} = -(V_1 + V_2 + V_3)$$

Thus, when the gain of summing amplifier is unity, the output voltage is the algebraic sum of the input voltages.

Summing Amplifier

Summing amplifier with gain greater than unity. When R_f is larger than the input resistors, the amplifer has a gain of R_f/R where R is the value of each input resistor. The general expression for the output voltage is

$$V_{out} = -\frac{R_f}{R}(V_1 + V_2 + V_3 + \ldots)$$

As you can see, the output voltage is the sum of input voltages multiplied by a constant determined by the ratio R_f/R.

Example 25.44. *Determine the output voltage for the summing amplifier in Fig. 25.72.*

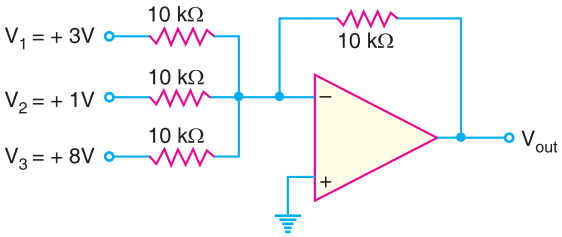


Fig. 25.72

Solution. Referring to Fig. 25.72, all the three input resistor values are equal and each is equal to the value of feedback resistor. Therefore, the gain of the summing amplifier is 1. As a result, the output voltage is the algebraic sum of three input voltages.

$$\therefore \quad V_{out} = -(V_1 + V_2 + V_3) = -(3 + 1 + 8) = \mathbf{-12\ V}$$

Example 25.45. *Determine the output voltage for the summing amplifier shown in Fig. 25.73.*

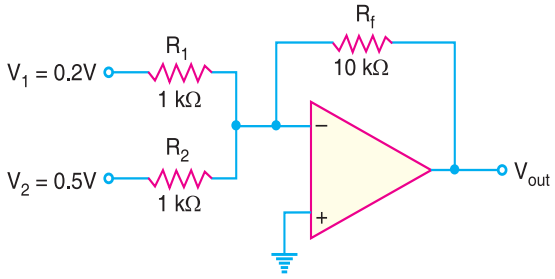


Fig. 25.73

Solution. $R_f = 10\ k\Omega$ and $R_1 = R_2 = R = 1\ k\Omega$. Therefore, gain of the amplifier $= -R_f/R = -10\ k\Omega/1k\Omega = -10$.

Now $$V_{out} = -\frac{R_f}{R}(V_1 + V_2) = -\frac{10\ k\Omega}{1k\Omega}(0.2 + 0.5) = \mathbf{-7V}$$

Note that the output voltage is not equal to the sum of input voltages. Rather it is equal to the sum of input voltages multiplied by the amplifier gain. In other words, the output voltage is proportional to the sum of the input voltages.

Example 25.46. *Determine the output voltage for the summing amplifier shown in Fig. 25.74.*

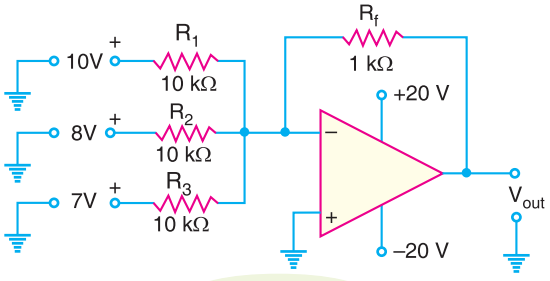


Fig. 25.74

Solution. $R_f = 1\ k\Omega$ and $R_1 = R_2 = R_3 = R = 10\ k\Omega$. Therefore, gain of the amplifier $= -R_f/R = -1\ k\Omega/10\ k\Omega = -1/10$.

Now
$$V_{out} = -\frac{R_f}{R}(V_1 + V_2 + V_3) = -\frac{1\ k\Omega}{10\ k\Omega}(10 + 8 + 7) = \mathbf{-2.5\ V}$$

Note that output voltage of the amplifier is not equal to the sum of input voltages, but rather is proportional to the sum of input voltages. In this case, it is equal to one-tenth of the input sum. Picking random values of V_1, V_2 and V_3 will show that this circuit always provides an output voltage that is one-tenth of the sum of input voltages.

Example 25.47. *Two voltages of + 0.6V and – 1.4 V are applied to the two input resistors of a summing amplifier. The respective input resistors are 400 kΩ and 100 kΩ and feedback resistor is 200 kΩ. Determine the output voltage.*

Solution. The output voltage of the summing amplifier is given by:
$$V_{out} = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)$$

Here $R_f = 200\ k\Omega$; $R_1 = 400\ k\Omega$; $R_2 = 100\ k\Omega$; $V_1 = +0.6V$; $V_2 = -1.4$ V

$\therefore$
$$V_{out} = -200\ k\Omega\left(\frac{0.6}{400\ k\Omega} + \frac{-1.4}{100\ k\Omega}\right) = \mathbf{2.5\ V}$$

Note that a summing amplifier produces an output voltage that is proportional to the *algebraic sum of* the input voltages.

Example 25.48. *Determine the output voltage from the circuit shown in Fig. 25.75 for each of the following input combinations*:

V_1(V)	V_2(V)	V_3(V)
+ 10	0	+10
0	+10	+10
+10	+10	+10

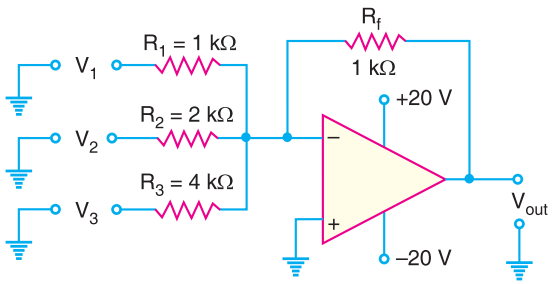


Fig. 25.75

Solution. The output voltage from the circuit is given by:
$$V_{out} = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$
$$= -\left(\frac{1k\Omega}{1\ k\Omega}V_1 + \frac{1k\Omega}{2\ k\Omega}V_2 + \frac{1k\Omega}{4\ k\Omega}V_3\right)$$

$\therefore$
$$V_{out} = -(V_1 + 0.5\ V_2 + 0.25\ V_3)$$

The output voltage for the first set of inputs is

$$V_{out} = -(10 + 0.5 \times 0 + 0.25 \times 10) = \mathbf{-12.5\ V}$$

The output voltage for the second set of inputs is

$$V_{out} = -(0 + 0.5 \times 10 + 0.25 \times 10) = \mathbf{-7.5\ V}$$

The output voltage for the third set of inputs is

$$V_{out} = -(10 + 0.5 \times 10 + 0.25 \times 10) = \mathbf{-17.5\ V}$$

Example 25.49. *Calculate the output voltage for the circuit of Fig. 25.76. The inputs are V_1 = 50 sin (1000 t)mV and V_2 = 10 sin (3000t) mV.*

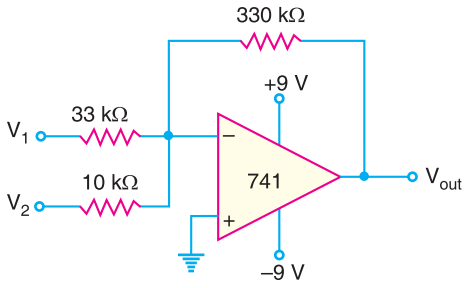


Fig. 25.76

Solution. The output voltage for the circuit is

$$V_{out} = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2\right) = -\left(\frac{330k\Omega}{33k\Omega}V_1 + \frac{330k\Omega}{10k\Omega}V_2\right)$$

$$= -(10\,V_1 + 33\,V_2) = -[10 \times 50 \sin(1000t) + 33 \times 10 \sin(3000t)]\ \text{mV}$$

$$= \mathbf{-[0.5 \sin (1000\,t) + 0.33 \sin (3000t)]\ V}$$

25.33 Applications of Summing Amplifiers

By proper modifications, a summing amplifier can be made to perform many useful functions. There are a number of applications of summing amplifiers. However, we shall discuss the following two applications by way of illustration:

1. As averaging amplifier
2. As subtractor

1. As averaging amplifier. By using the proper input and feedback resistor values, a summing amplifier can be designed to provide an output voltage that is equal to the *average* of input voltages. A summing amplifier will act as an averaging amplifier when *both* of the following conditions are met:

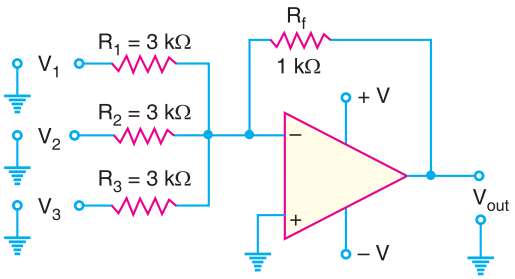


Fig. 25.77

(i) All input resistors (R_1, R_2 and so on) are *equal in value.*

(ii) The ratio of any input resistor to the feedback resistor is equal to the number of input circuits.

Fig. 25.77 shows the circuit of averaging amplifier. Note that it is a summing amplifier meeting the above two conditions. All input resistors are equal in value (3 kΩ). If we take the ratio of any input resistor to the feedback resistor, we get 3 kΩ/ 1 kΩ = 3. This is equal to the number of inputs to the circuit. Referring to the circuit in Fig. 25.77, the output voltage is given by;

$$V_{out} = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

Now $$\frac{R_f}{R_1} = \frac{R_f}{R_2} = \frac{R_f}{R_3} = \frac{1\,\text{k}\Omega}{3\,\text{k}\Omega} = \frac{1}{3}$$

$\therefore$ $$V_{out} = -\left(\frac{V_1 + V_2 + V_3}{3}\right)$$

Note that V_{out} is equal to the average of the three inputs. The negative sign shows the phase reversal.

2. As subtractor. A summing amplifier can be used to provide an output voltage that is equal to the difference of two voltages. Such a circuit is called a **subtractor** and is shown in Fig. 25.78. As we shall see, this circuit will provide an output voltage that is equal to the difference between V_1 and V_2.

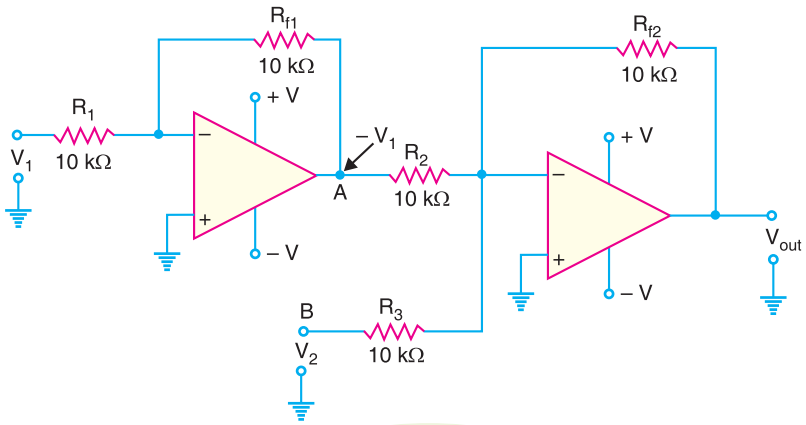


Fig. 25.78

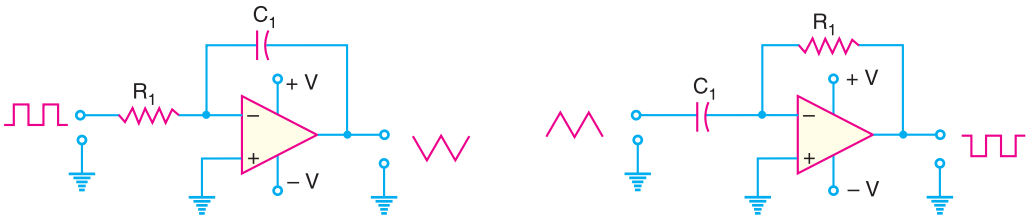
The voltage V_1 is applied to a standard inverting amplifier that has *unity gain.* Because of this, the output from the inverting amplifier will be equal to $-V_1$. This output is then applied to the summing amplifier (also having unity gain) along with V_2. Thus output from second *OP*-amp is given by;

$$V_{out} = -(V_A + V_B) = -(-V_1 + V_2) = V_1 - V_2$$

It may be noted that the gain of the second stage in the subtractor can be varied to provide an output that is proportional to (rather than equal to) the difference between the input voltages. However, if the circuit is to act as a subtractor, the input inverting amplifier *must* have unity gain. Otherwise, the output will not be proportional to the true difference between V_1 and V_2.

25.34 OP-Amp Integrators and Differentiators

A circuit that performs the mathematical integration of input signal is called an *integrator.* The output of an integrator is proportional to the area of the input waveform over a period of time. A circuit that performs the mathematical differentiation of input signal is called a *differentiator.* The output of a differentiator is proportional to the rate of change of its input signal. Note that the two operations are opposite.



OP-amp Integrator (*i*) *OP*-amp differentiator (*ii*)

Fig. 25.79

Fig.25.79 shows *OP*-amp integrator and differentiator. As you can see, the two circuits are nearly identical in terms of their construction. Each contains a single *OP*-amp and an *RC* circuit. However, the difference in resistor/capacitor placement in the two circuits causes them to have input/output relationships that are exact opposites. For example, if the input to the integrator is a square wave, the output will be a triangular wave as shown in Fig. 25.79 (*i*). However, the differentiator will convert a triangular wave into square wave as shown in Fig. 25.79 (*ii*).

25.35 *OP*-Amp Integrator

As discussed above, an integrator is a circuit that performs integration of the input signal. The most popular application of an integrator is to produce a *ramp* output voltage (*i.e.* a linearly increasing or decreasing voltage). Fig. 25.80 shows the circuit of an *OP*-amp integrator. It consists of an *OP*-amp, input resistor *R* and feedback capacitor *C*. Note that the feedback component is a capacitor instead of a resistor.

As we shall see, when a signal is applied to the input of this circuit, the output-signal waveform will be the integration of input-signal waveform.

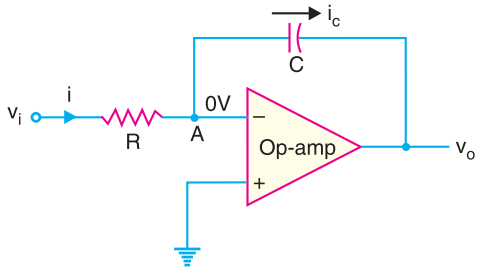


Fig. 25.80

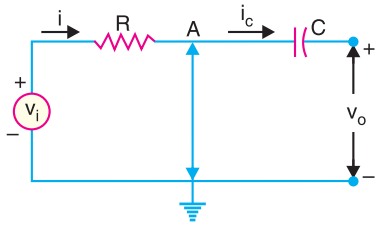


Fig. 25.81

Circuit Analysis. Since point *A* in Fig. 25.80 is at virtual ground, the *virtual-ground equivalent circuit of operational integrator will be as shown in Fig. 25.81. Because of virtual ground and infinite impedance of the *OP*-amp, all of the input current *i* flows through the capacitor *i.e.* $i = i_c$.

Now
$$i = \frac{v_i - 0}{R} = \frac{v_i}{R} \qquad ...(i)$$

Also voltage across capacitor is $v_c = 0 - v_o = -v_o$

$\therefore$
$$i_c = \frac{C\,dv_c}{dt} = -C\frac{dv_o}{dt} \qquad ...(ii)$$

* Recall that virtual ground means that point *A* is 0V but it is not mechanically grounded. Therefore, no current flows from point *A* to ground.

From eqs. (*i*) and (*ii*), $\frac{v_i}{R} = -C\frac{dv_o}{dt}$

or $\frac{dv_o}{dt} = -\frac{1}{RC}v_i$ ...(*iii*)

To find the output voltage, we integrate both sides of eq. (*iii*) to get,

$$v_o = -\frac{1}{RC}\int_0^t v_i\,dt \qquad ...(iv)$$

Eq. (*iv*) shows that the output is the integral of the input with an inversion and scale multiplier of $1/RC$.

Output voltage. If a fixed voltage is applied to the input of an integrator, eq. (*iv*) shows that the output voltage grows over a period of time, providing a ramp voltage. Eq. (*iv*) also shows that the output voltage ramp (for a fixed input voltage) is opposite in polarity to the input voltage and is multiplied by the factor $1/RC$. As an example, consider an input voltage $v_1 = 1$V to the integrator circuit of Fig. 25.82 (*i*). The scale factor of $1/RC$ is

$$-\frac{1}{RC} = -\frac{1}{(1\,\text{M}\Omega)\,(1\mu\text{F})} = -1$$

so that the output is a negative ramp voltage as shown in Fig. 25.82 (*ii*).

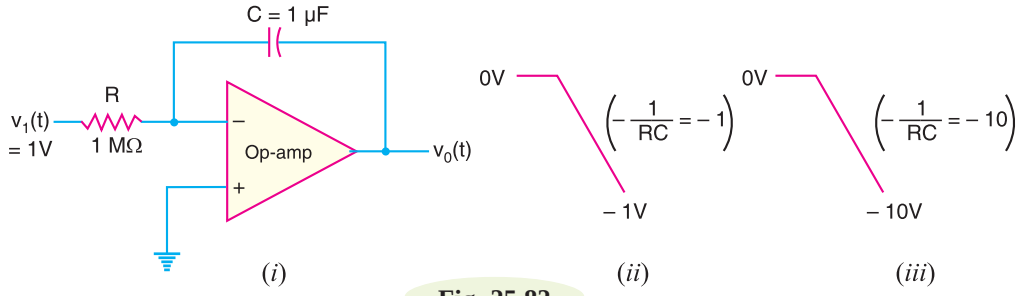


Fig. 25.82

If the scale factor is changed by making $R = 100$ kΩ, then,

$$-\frac{1}{RC} = -\frac{1}{(100\,\text{k}\Omega)\,(1\mu\text{F})} = -10$$

and output is then a steeper ramp voltage as shown in Fig. 25.82 (*iii*).

25.36 Critical Frequency of Integrators

The integrator shown in Fig. 25.80 (Refer back) has no feedback at 0 Hz. This is a serious disadvantage in low-frequency applications. By connecting a feedback resistor R_f in parallel with the capacitor, precise closed-loop voltage gain is possible. The circuit shown in Fig. 25.83 is an integrator with a feedback resistor R_f to provide increased stability.

All integrators have a critical frequency f_c below which they do not perform proper integration. If the input frequency is less than f_c, the circuit behaves like a simple inverting amplifier and no integration occurs. The following equation is used to calculate the critical frequency of an integrator:

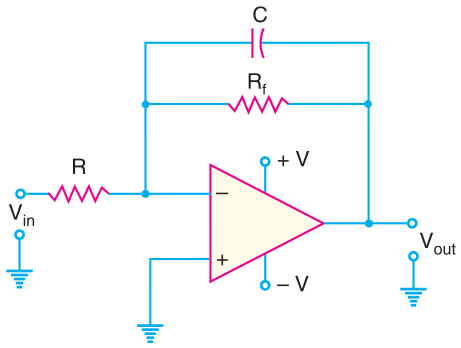
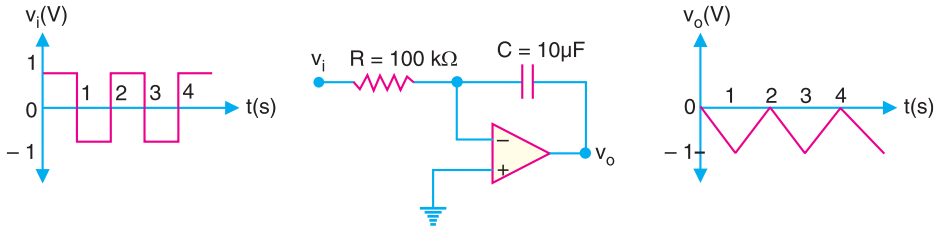


Fig. 25.83

$$f_c = \frac{1}{2\pi R_f C}$$

Example 25.50. *Fig. 25.84 (i) shows the OP-amp integrator and the square wave input. Find the output voltage.*



(*i*) (*ii*)

Fig. 25.84

Solution. The output voltage of this circuit is given by;

$$v_o = -\frac{1}{RC}\int_0^t v_i\, dt$$

Now $RC = (100\ \text{k}\Omega)\ (10\ \mu\text{F}) = (100 \times 10^3\Omega)\ (10 \times 10^{-6}\ \text{F}) = 1\text{s}$

$\therefore$ $$v_o = -\int_0^t v_i\, dt$$

When we integrate a constant, we get a straight line. In other words, when input voltage to an integrator is constant, the output is a linear ramp. Therefore, the integration of the square wave results in the triangular wave as shown in Fig. 25.84 (*ii*). Since the input to the integrator is applied to the inverting input, the output of the circuit will be 180° out of phase with the input. Thus, when the input goes positive, the output will be a negative ramp. When the input is negative, the output will be a positive ramp. Fig. 25.84 (*ii*) shows this relationship.

Example 25.51. *Determine the lower frequency limit (critical frequency) for the integrator circuit shown in Fig. 25.85.*

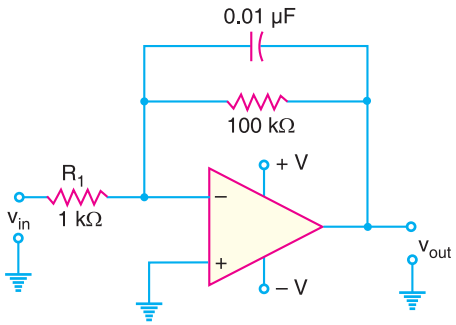


Fig. 25.85

Solution. The critical frequency for the integrator circuit shown in Fig. 25.85 is given by;

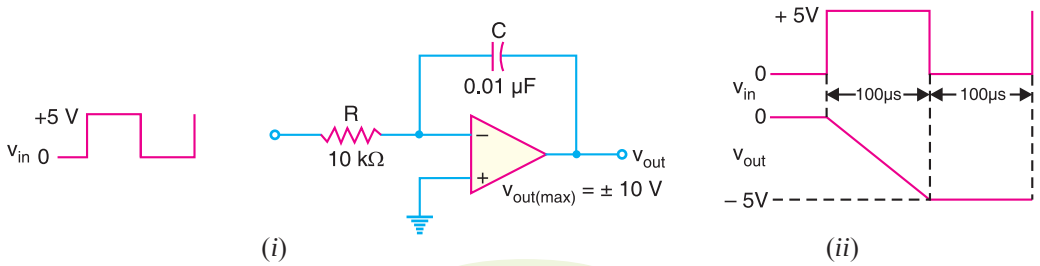
$$f_c = \frac{1}{2\pi R_f C}$$

Here $R_f = 100\ \text{k}\Omega = 10^5\Omega$; $C = 0.01\ \mu\text{F} = 0.01 \times 10^{-6}\ \text{F}$

$$\therefore \quad f_c = \frac{1}{2\pi \times (10^5) \times (0.01 \times 10^{-6})} = \mathbf{159\ Hz}$$

Example 25.52. (*i*) *Determine the rate of change of the output voltage in response to a single pulse input to the integrator circuit shown in Fig. 25.86 (i).*

(*ii*) *Draw the output waveform.*



(*i*) (*ii*)

Fig. 25.86

Solution.

(*i*) Output voltage, $v_{out} = -\frac{1}{RC}\int_0^t v_{in}\, dt$

Therefore, the rate of change of output voltage is

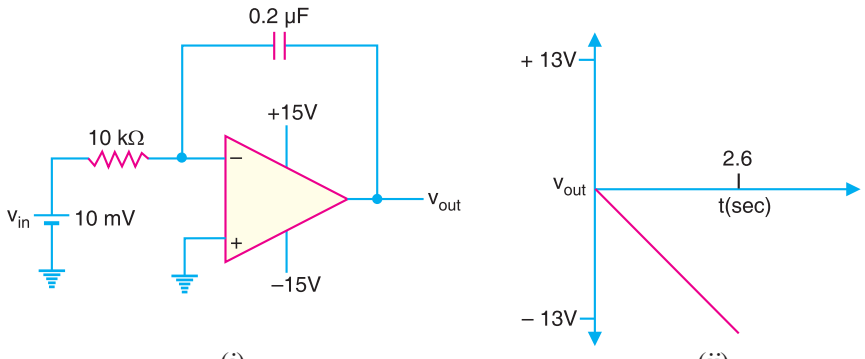
$$\frac{\Delta v_{out}}{dt} = -\frac{v_{in}}{RC} = -\frac{5\text{ V}}{(10\text{ k}\Omega)\,(0.01\,\mu\text{F})} = -50\text{ kV/s} = \mathbf{-50\ mV/\mu s}$$

(*ii*) The rate of change of output voltage is – 50 mV/μs. When the input is at + 5 V, the output is a negative-going ramp. When the input is at 0 V, the output is a constant level. In 100 μs, the output voltage decreases.

$$\therefore \quad \Delta v_{out} = \frac{\Delta v_{out}}{dt} \times dt = -\frac{50\text{ mV}}{\mu\text{s}} \times 100\,\mu\text{s} = -5\text{V}$$

Therefore, the negative-going ramp reaches – 5 V at the end of the pulse (*i.e.* after 100 μs from the initial condition). The output voltage then remains constant at – 5 V for the time the input is zero. Fig. 25.86 (*ii*) shows the output waveform.

Example 25.53. *For the integrator circuit shown in Fig. 25.87 (i), how long does it take for the output to reach saturation ?*



(*i*) (*ii*)

Fig. 25.87

Solution.

$$\text{Output voltage, } v_{out} = -\frac{1}{RC}\int_0^t v_{in}\,dt$$

Since the input voltage v_{in} (= 10 mV) is constant,

$$\therefore \quad v_{out} = -\frac{1}{RC}v_{in}t = -\frac{1}{(10\ k\Omega)\,(0.2\ \mu F)} \times (10\ mV) \times t$$

$$\text{or} \quad v_{out} = -5t \text{ volts}$$

$$\text{Now} \quad \text{Saturation voltage, } V_s = -V_{supply} + 2 = -15 + 2 = -13 \text{ V}$$

$$\therefore \quad \text{Time required, } t = \frac{V_s}{-5} = \frac{-13}{-5} = \textbf{2.6 seconds}$$

Fig. 25.87 (*ii*) shows the output waveform.

25.37 OP-Amp Differentiator

A differentiator is a circuit that performs differentiation of the input signal. In other words, a differentiator produces an output voltage that is proportional to the rate of change of the input voltage. Its important application is to produce a rectangular output from a ramp input. Fig. 25.88 shows the circuit of OP-amp differentiator. It consists of an OP-amp, an input capacitor *C* and feedback resistor *R*. Note how the placement of the capacitor and resistor differs from the integrator. The capacitor is now the input element.

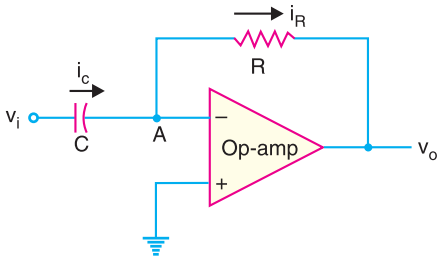


Fig. 25.88

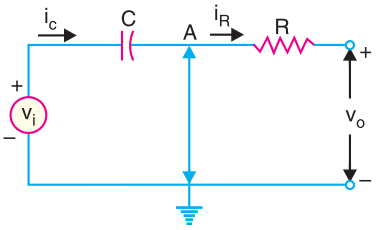


Fig. 25.89

Circuit analysis. Since point *A* in Fig. 25.88 is at virtual ground, the virtual-ground equivalent circuit of the operational differentiator will be as shown in Fig. 25.89. Because of virtual ground and infinite impedance of OP-amp, all the input current i_c flows through the feedback resistor *R i.e.* $i_c = i_R$.

$$\therefore \quad i_R = \frac{0 - v_o}{R} = -\frac{v_o}{R} \quad \text{and} \quad v_c = v_i - 0 = v_i$$

$$\text{Also} \quad i_c = C\frac{dv_c}{dt} = C\frac{dv_i}{dt}$$

$$\therefore \quad -\frac{v_o}{R} = C\frac{dv_i}{dt} \qquad (\because\ i_R = i_c)$$

$$\text{or} \quad v_o = -RC\frac{dv_i}{dt} \qquad \ldots(i)$$

Eq. (*i*) shows that output is the differentiation of the input with an inversion and scale multiplier of *RC*. If we examine eq. (*i*), we see that if the input voltage is constant, dv_i/dt is zero and the output voltage is zero. The faster the input voltage changes, the larger the magnitude of the output voltage.

Example 25.54. *Fig. 25.90 (i) shows the square wave input to a differentiator circuit. Find the output voltage if input goes from 0V to 5V in 0.1 ms.*

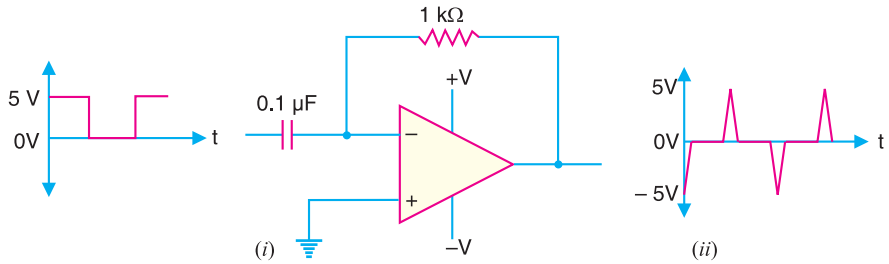


Fig. 25.90

Solution. Output voltage, $v_o = -RC\frac{dv_i}{dt}$

Now, $RC = (1\,\text{k}\Omega)\times(0.1\,\mu\text{F}) = (10^3\,\Omega)(0.1\times10^{-6}\,\text{F}) = 0.1\times10^{-3}\,s$

Also, $\frac{dv_i}{dt} = \frac{5\text{V}}{0.1\,\text{ms}} = \frac{5\times10^4\,\text{V}}{s} = 5\times10^4\,\text{V/s}$

$\therefore \quad v_o = -(0.1\times10^{-3})(5\times10^4) = \mathbf{-5V}$

The signal quickly returns to zero as the input signal becomes constant. The output will be as shown in Fig. 25.90 (*ii*).

Example 25.55. *For the differentiator circuit shown in Fig. 25.91, determine the output voltage if the input goes from 0V to 10V in 0.4s. Assume the input voltage changes at constant rate.*

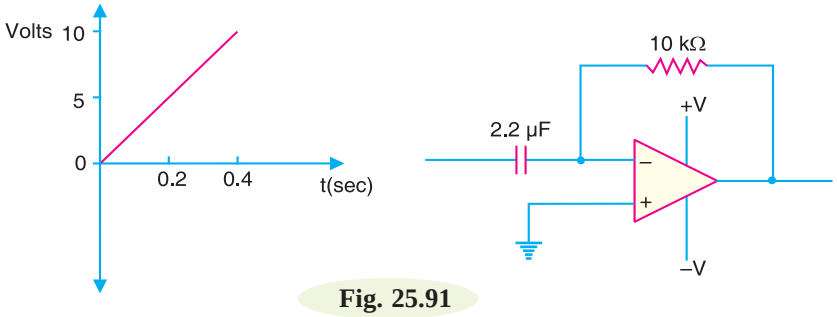


Fig. 25.91

Solution. Output voltage, $v_o = -RC\frac{dv_i}{dt}$

Now, $RC = (10\,\text{k}\Omega)\times(2.2\,\mu\text{F}) = (10^4\,\Omega)(2.2\times10^{-6}\,\text{F}) = 2.2\times10^{-2}\,s$

Also, $\frac{dv_i}{dt} = \frac{(10-0)\,V}{0.4s} = \frac{10\text{V}}{0.4\text{s}} = 25\,\text{V/s}$

$\therefore \quad v_o = -(2.2\times10^{-2})\times25 = \mathbf{-0.55\ V}$

The output voltage stays constant at – 0.55 V.

Example 25.56. *For the differentiator circuit shown in Fig. 25.92(i), determine (i) the expression for the output voltage (ii) the output voltage for the given input.*

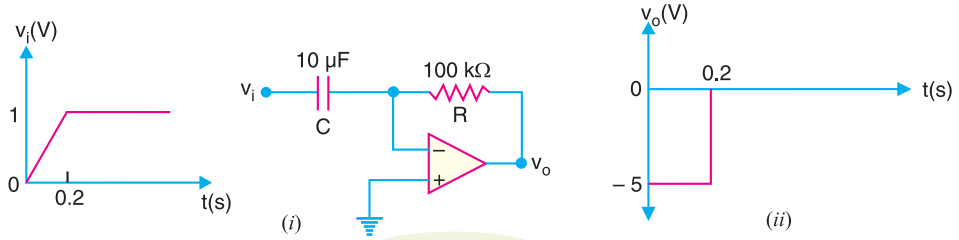


Fig. 25.92

Solution.

(*i*) For the differentiator shown in Fig. 25.92 (*i*), the output voltage is given by;

$$v_o = -RC\frac{dv_i}{dt} = -(100\,\text{k}\Omega)\times(10\,\mu\text{F})\frac{dv_i}{dt}$$

$$= -(100\times10^3\,\Omega)\times(10\times10^{-6}\,\text{F})\frac{dv_i}{dt} = \mathbf{-\frac{dv_i}{dt}}$$

(*ii*) Since the input voltage is a straight line between 0 and 0.2*s*, the output voltage is

$$v_o = -\frac{dv_i}{dt} = -\frac{(1-0)}{0.2} = \mathbf{-5V}$$

Therefore, between 0 to 0.2*s*, the output voltage is constant at – 5 V. For $t > 0.2s$, the input is constant so that output voltage is zero. Fig. 25.92 (*ii*) shows the output waveform.

25.38. Comparators

Often we want to compare one voltage to another to see which is larger. In this situation, a *comparator* may be used. A *comparator is an OP-amp circuit without negative feedback* and takes advantage of very high open-loop voltage gain of OP-amp. A comparator has two input voltages (noninverting and inverting) and one output voltage. Because of the high open-loop voltage gain of an *OP*-amp, a very small difference voltage between the two inputs drives the amplifier to saturation. For example, consider an *OP*-amp having A_{OL} = 100,000. A voltage difference of only 0.25 mV between the inputs will produce an output voltage of (0.25 mV) (100,000) = 25V. However, most of OP-amps have output voltages of less than ± 15V because of their d.c. supply voltages. Therefore, a very small differential input voltage will drive the OP-amp to saturation. This is the key point in the working of comparator.

Fig. 25.93 illustrates the action of a comparator. The input voltages are v_1 (signal) and v_2 (*reference voltage). If the differential input is positive, the circuit is driven to saturation and output goes to maximum positive value (**$+V_{sat} = +13$V). Reverse happens when the differential input goes negative *i.e.* now output is maximum negative ($-V_{sat} = -13$V). This circuit is called comparator because it compares v_1 to v_2 to produce a saturated positive or negative output voltage. Note that output voltage rapidly changes from – 13V to + 13V and *vice-versa*.

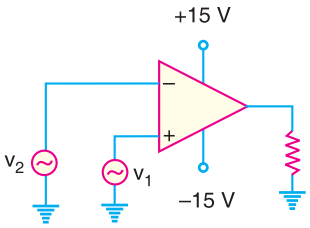


Fig. 25.93

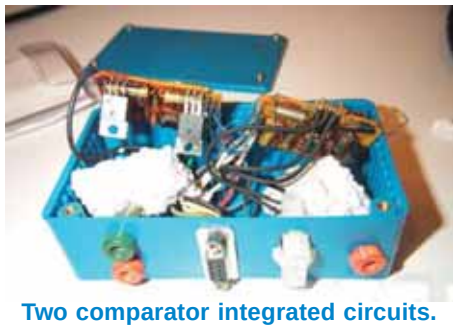
25.39 Comparator Circuits

A comparator circuit has the following two characteristics :

(*i*) It uses no feedback so that the voltage gain is equal to the open-loop voltage gain (A_{OL}) of *OP*-amp.

(*ii*) It is operated in a non-linear mode.

These properties of a comparator permit it to perform many useful functions.



Two comparator integrated circuits.

* If this terminal is grounded, $v_2 = 0$V.

** Since in our case supply voltages are ± 15V,

$$+V_{sat} = +V_{supply} - 2 = 15 - 2 = +13\text{V}$$

$$-V_{sat} = -V_{supply} + 2 = -15 + 2 = -13\text{V}$$

1. As a square wave generator. A comparator can be used to produce a square wave output from a sine wave input. Fig. 25.94 shows the circuit of a comparator to produce square wave output. Note that inverting terminal (–) is grounded and signal (v_{in}) is applied to the noninverting terminal (+). Since the gain of a comparator is equal to A_{OL}, virtually any difference voltage at the inputs will cause the output to go to one of the voltage extremes (+ V_{sat} or – V_{sat}) and stay there until the voltage difference is removed. The polarity of the input difference voltage will determine to which extreme (+V_{sat} or – V_{sat}) the output of the comparator goes.

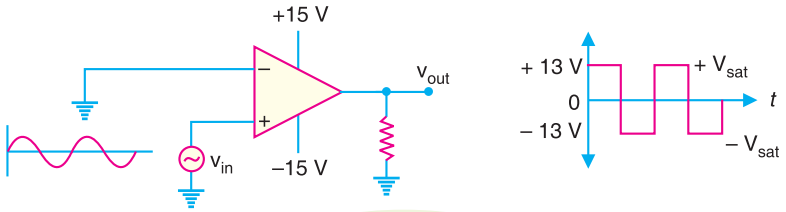


Fig. 25.94

When the input signal goes positive, the output jumps to about + 13 V. When the input goes negative, the output jumps to about – 13 V. The output changes rapidly from – 13 V to + 13 V and *vice-versa*. This change is so rapid that we get a square wave output for a sine wave input.

2. As a zero-crossing detector. When one input of a comparator is connected to ground, it is known as zero-crossing detector because the output changes when the input crosses 0 V. The zero-crossing circuit is shown in Fig. 25.95. The input and output waveforms are also shown. When the input signal is positive-going, the output is driven to positive maximum value (*i.e.* + V_{sat} = + 13 V). When the input crosses the zero axis and begins to go negative, the output is driven to negative maximum value (*i.e.* – V_{sat} = – 13 V).

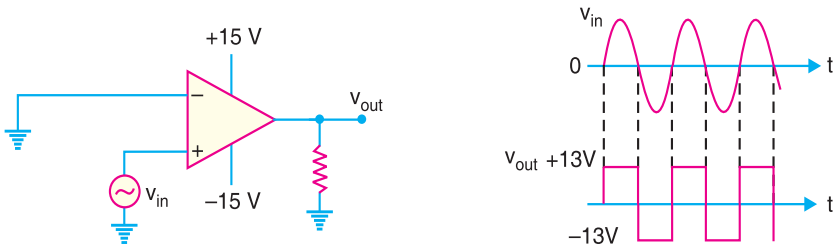


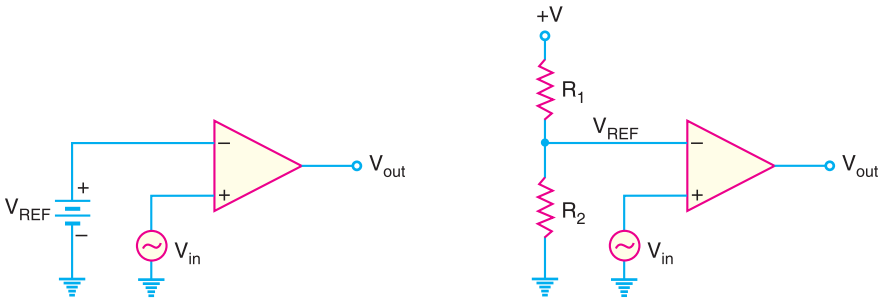
Fig. 25.95

From the input/output waveforms, you can see that every time the input crosses 0 V going positive, the output jumps to + 13 V. Similarly, every time the input crosses 0 V going negative, the output jumps to – 13 V. Since the change (+ 13 V or – 13 V) occurs every time the input crosses 0 V, we can tell when the input signal has crossed 0 V. Hence the name zero-crossing detector.

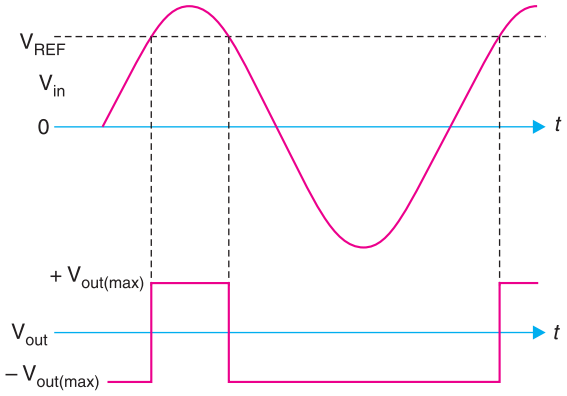
3. As a level detector. When a comparator is used to compare a signal amplitude to a fixed d.c. level (reference voltage), the circuit is referred to as a level detector. We can modify zero-crossing detector circuit to construct level detector. This can be done by connecting a fixed reference voltage V_{REF} to the inverting input as shown in Fig. 25.96 (*i*). A more practical arrangement is shown in Fig. 25.96 (*ii*) using a voltage divider to set the reference voltage as follows :

$$V_{REF} = \frac{R_2}{R_1 + R_2}(+V)$$

where + V is the positive *OP*-amp d.c. supply voltage.



(*i*) Battery reference (*ii*) Voltage-divider reference



(*iii*) Waveforms

Fig. 25.96

The circuit action is as follows. Suppose the input signal v_{in} is a sine wave. When the input voltage is less than the reference voltage (*i.e.* $V_{in} < V_{REF}$), the output goes to maximum negative level. It remains here until V_{in} increases above V_{REF}. When the input voltage exceeds the reference voltage (*i.e.* $V_{in} > V_{REF}$), the output goes to its maximum positive state. It remains here until V_{in} decreases below V_{REF}. Fig. 25.96 (*iii*) shows the input/output waveforms. Note that this circuit is used for non zero-level detection.

MULTIPLE-CHOICE QUESTIONS

1. A differential amplifier .....
- (*i*) is a part of an OP-amp
- (*ii*) has one input and one output
- (*iii*) has two outputs
- (*iv*) answers (*i*) and (*iii*)

2. When a differential amplifier is operated single-ended, ...
- (*i*) the output is grounded
- (*ii*) one input is grounded and signal is applied to the other
- (*iii*) both inputs are connected together
- (*iv*) the output is not inverted

3. In differential-mode, ...
- (*i*) opposite polarity signals are applied to the inputs
- (*ii*) the gain is one
- (*iii*) the outputs are of different amplitudes
- (*iv*) only one supply voltage is used

4. In the common-mode, ...
- (*i*) both inputs are grounded
- (*ii*) the outputs are connected together
- (*iii*) an identical signal appears on both inputs
- (*iv*) the output signals are in-phase

5. The common-mode gain is ....
(*i*) very high (*ii*) very low
(*iii*) always unity (*iv*) unpredictable

6. The differential gain is ....
(*i*) very high (*ii*) very low
(*iii*) dependent on input voltage
(*iv*) about 100

7. If $A_{DM} = 3500$ and $A_{CM} = 0.35$, the *CMRR* is ....
(*i*) 1225
(*ii*) 10,000
(*iii*) 80 *dB*
(*iv*) answers (*ii*) and (*iii*)

8. With zero volts on both inputs, an OP-amp ideally should have an output ....
(*i*) equal to the positive supply voltage
(*ii*) equal to the negative supply voltage
(*iii*) equal to zero
(*iv*) equal to the *CMRR*

9. Of the values listed, the most realistic value for open-loop voltage gain of an OP-amp is ....
(*i*) 1 (*ii*) 2000
(*iii*) 80 *dB* (*iv*) 100,000

10. A certain OP-amp has bias currents of 50 μA and 49.3 μA. The input offset current is ....
(*i*) 700 n*A* (*ii*) 99.3 μ*A*
(*iii*) 49.7 μ*A* (*iv*) none of these

11. The output of a particular OP-amp increases 8 V in 12 μs. The slew rate is ....
(*i*) 90 V/μs (*ii*) 0.67 V/μs
(*iii*) 1.5 V/μs (*iv*) none of these

12. For an OP-amp with negative feedback, the output is ....
(*i*) equal to the input
(*ii*) increased
(*iii*) fed back to the inverting input
(*iv*) fed back to the noninverting input

13. The use of negative feedback ....
(*i*) reduces the voltage gain of an OP-amp
(*ii*) makes the OP-amp oscillate
(*iii*) makes linear operation possible
(*iv*) answers (*i*) and (*iii*)

14. Negative feedback ....
(*i*) increases the input and output impedances
(*ii*) increases the input impedance and bandwidth
(*iii*) decreases the output impedance and bandwidth
(*iv*) does not affect impedance or bandwidth

15. A certain noninverting amplifier has R_i of 1 kΩ and R_f of 100 kΩ. The closed-loop voltage gain is ....
(*i*) 100,000 (*ii*) 1000
(*iii*) 101 (*iv*) 100

16. If feedback resistor in *Q*.15 is open, the voltage gain .....
(*i*) increases (*ii*) decreases
(*iii*) is not affected (*iv*) depends on R_i

17. A certain inverting amplifier has a closed-loop voltage gain of 25. The OP-amp has an open-loop voltage gain of 100,000. If an OP-amp with an open-loop voltage gain of 200,000 is substituted in the arrangement, the closed-loop gain .....
(*i*) doubles (*ii*) drops to 12.5
(*iii*) remains at 25 (*iv*) increases slightly

18. A voltage follower ....
(*i*) has a voltage gain of 1
(*ii*) in noninverting
(*iii*) has no feedback resistor
(*iv*) has all of these

19. The OP-amp can amplify ....
(*i*) a.c. signals only
(*ii*) d.c. signals only
(*iii*) both a.c. and d.c. signals
(*iv*) neither d.c. nor a.c. signals

20. The input offset current equals the ....
(*i*) difference between two base currents
(*ii*) average of two base currents
(*iii*) collector current divided by current gain
(*iv*) none of these

21. The tail current of a differential amplifier is ....
(*i*) half of either collector current

(*ii*) equal to either collector current
(*iii*) two times either collector current
(*iv*) equal to the difference in base currents

22. The node voltage at the top of the tail resistor is closest to ....
(*i*) collector supply voltage
(*ii*) zero
(*iii*) emitter supply voltage
(*iv*) tail current times base resistance

23. The tail current in a differential amplifier equals ....
(*i*) difference between two emitter currents
(*ii*) sum of two emitter currents
(*iii*) collector current divided by current gain
(*iv*) collector voltage divided by collector resistance

24. The differential voltage gain of a differential amplifier is equal to R_C divided by ....
(*i*) r'_e (*ii*) $r'_e/2$
(*iii*) $2\,r'_e$ (*iv*) R_E

25. The input impedance of a differential amplifier equals r'_e times ....
(*i*) β (*ii*) R_E
(*iii*) R_C (*iv*) 2β

26. A common-mode signal is applied to ....
(*i*) the noninverting input
(*ii*) the inverting input
(*iii*) both inputs
(*iv*) top of the tail resistor

27. The common-mode voltage gain is ....
(*i*) smaller than differential voltage gain
(*ii*) equal to differential voltage gain
(*iii*) greater than differential voltage gain
(*iv*) none of the above

28. The input stage of an OP-amp is usually a ....
(*i*) differential amplifier
(*ii*) class *B* push-pull amplifier
(*iii*) *CE* amplifier
(*iv*) swamped amplifier

29. The common-mode voltage gain of a differential amplifier is equal to R_C divided by ....
(*i*) r'_e (*ii*) $2\,r'_e$
(*iii*) $r'_e/2$ (*iv*) $2\,R_E$

30. Current cannot flow to ground through ....
(*i*) a mechanical ground
(*ii*) an a.c. ground
(*iii*) a virtual ground
(*iv*) an ordinary ground

Answers to Multiple-Choice Questions

1. (*iv*)	**2.** (*ii*)	**3.** (*i*)	**4.** (*iii*)	**5.** (*ii*)
6. (*i*)	**7.** (*iv*)	**8.** (*iii*)	**9.** (*iv*)	**10.** (*i*)
11. (*ii*)	**12.** (*iii*)	**13.** (*iv*)	**14.** (*ii*)	**15.** (*iii*)
16. (*i*)	**17.** (*iii*)	**18.** (*iv*)	**19.** (*iii*)	**20.** (*i*)
21. (*iii*)	**22.** (*ii*)	**23.** (*ii*)	**24.** (*iii*)	**25.** (*iv*)
26. (*iii*)	**27.** (*i*)	**28.** (*i*)	**29.** (*iv*)	**30.** (*iii*)

Chapter Review Topics

1. What is an operational amplifier (OP-amp)?
2. Give the block diagram of an operational amplifier.
3. What is a differential amplifier?
4. Draw the basic circuit of a differential amplifier.
5. Discuss the operation of a differential amplifier.
6. What do you mean by noninverting and inverting input of a differential amplifier?
7. What are common-mode and differential-mode signals?
8. What do you mean by *CMRR*?

9. What is the importance of *CMRR*?
10. Explain the d.c. analysis of a differential amplifier.
11. What do you mean by (*i*) output offset voltage (*ii*) input offset current?
12. Derive an expression for differential-mode voltage gain of a differential amplifier.
13. Derive an expression for the common-mode voltage gian of a differential amplifier.
14. Draw the schematic symbol of an operational amplifier indicating the various terminals.
15. What do you-mean by (*i*) open-loop voltage gain (*ii*) closed-loop voltage gain of an OP-amp?
16. Discuss OP-amp input/output polarity relationship.
17. What do you mean by bandwidth of an OP-amp?
18. What do you mean by slew rate of an OP-amp?
19. Discuss the frequency response of an OP-amp.
20. What is the need of negative feedback in an OP-amp?
21. Derive an expression for the voltage gain of an inverting amplifier.
22. Derive an expression for the voltage gain of a noninverting amplifier.
23. What is a voltage follower?
24. Draw the circuit of multistage OP-amp.
25. What is the effect of negative feedback on (*i*) noninverting amplifier (*ii*) inverting amplifier ?
26. Discuss the operation of a summing amplifier.
27. Discuss two applications of summing amplifiers.
28. Discuss the operation of an OP-amp integrator.
29. What is the most important application of an OP-amp integrator?
30. Discuss the operation of OP-amp differentiator.

Problems

1. In Fig 25.97, the transistors are identical with $\beta_{dc} = 200$. What is the output voltage? **[7.5 V]**

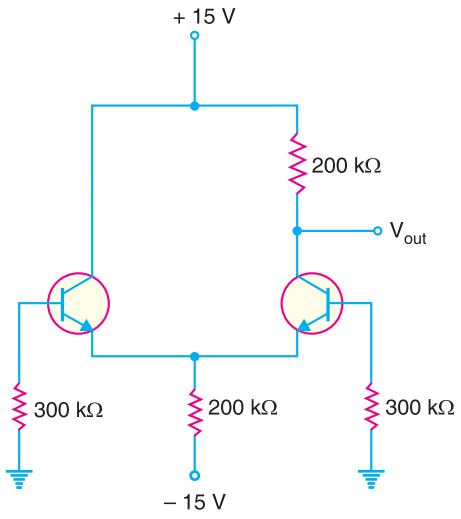


Fig. 25.97

2. In Fig. 25.97, the left transistor has $\beta_{dc} = 225$ and the right transistor has $\beta_{dc} = 275$. What are the base voltages? **[– 0.05 V ; – 0.0409 V]**
3. A data sheet gives an input bias current of 20 *nA* and an input offset current of 3 nA. What are the base currents? **[18.5 nA ; 21.5 nA]**
4. Find bias voltages and currents for the differential amplifier circuit in Fig. 25.98.

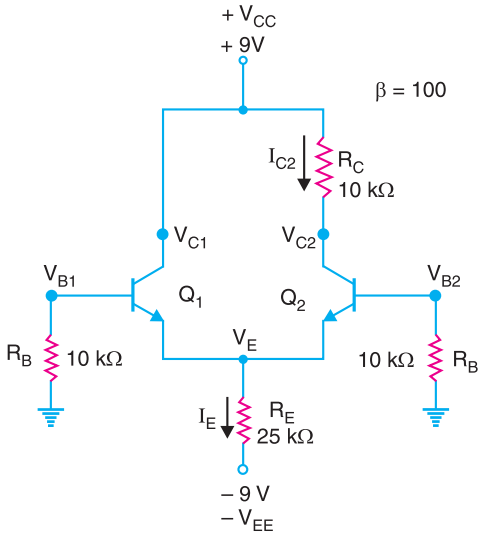


Fig. 25.98

[V_E = **– 0.7 V** ; I_E = **0.332 mA** ; $I_{E1} = I_{E2}$ = **0.166 mA** ; $I_{C1} = I_{C2}$ = **0.166 mA** ; $I_{B1} = I_{B2}$ = **1.66 μA**; V_{C1} = **9 V** ; V_{C2} = **7.34 V**]

5. Find the bias voltages and currents for the differential amplifier circuit shown in Fig. 25.99.

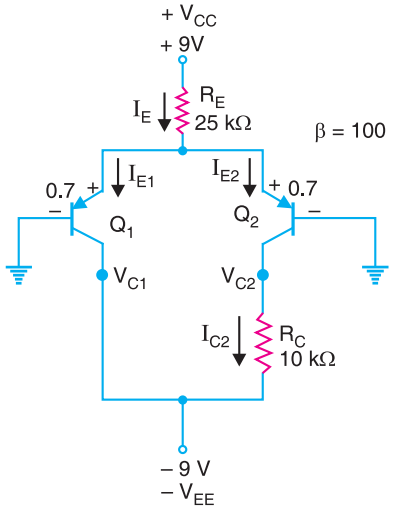


Fig. 25.99

[V_E = **0.7 V** ; I_E = **0.332 mA** ; $I_{E1} = I_{E2}$ = **0.166 mA** ; $I_{C1} = I_{C2}$ = **0.166 mA** ; $I_{B1} = I_{B2}$ = **1.66 μA**; V_{C1} = **– 9 V** ; V_{C2} = **– 7.34 V**]

6. For the circuit shown in Fig. 25.100, determine (*i*) common-mode voltage gain (*ii*) differential-mode voltage gain (*iii*) *CMRR*. **[(*i*) 0.42 (*ii*) 90.6 (*iii*) 216]**

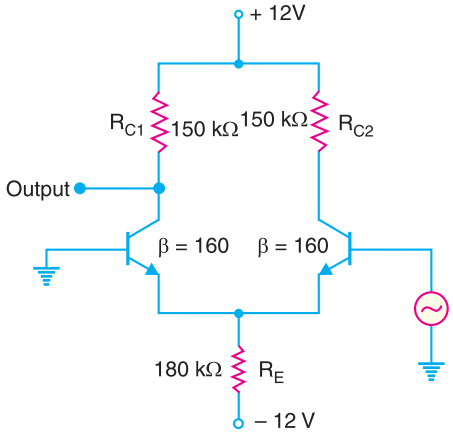


Fig. 25.100

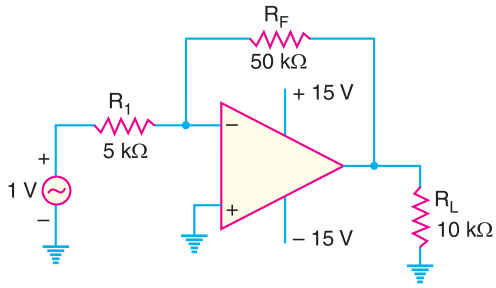


Fig. 25.101

7. For the circuit shown in Fig. 25.101, find (*i*) closed-loop voltage gain (*ii*) the instantaneous voltage across R_F when the signal voltage is + 1*V* (*iii*) the instantaneous voltage on the –terminal when the signal voltage is + 1*V*. **[(*i*) 10 (*ii*) 10 *V* (*iii*) 0 *V*]**

8. A noninverting amplifier has an R_i of 1 kΩ and an R_f of 100 kΩ. Determine (*i*) V_f (*ii*) feedback factor if V_{out} = 5 V. **[(*i*) 49.5 mV ; (*ii*) 9.9×10^{-3}]**

9. Determine the closed-loop voltage gain for the circuit shown in Fig. 25.102. **[11]**

10. Determine the closed-loop voltage gain for the circuit shown in Fig. 25.103. **[101]**

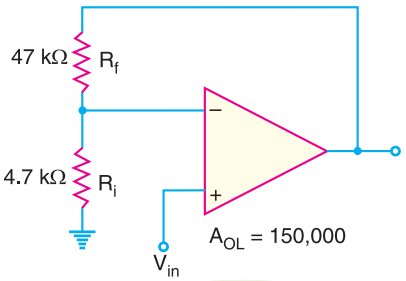


Fig. 25.102

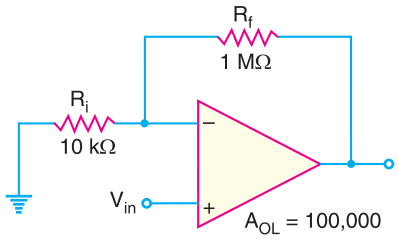


Fig. 25.103

11. Find the closed-loop voltage gain for each of the circuits shown in Fig. 25.104. **[1 ; – 1]**

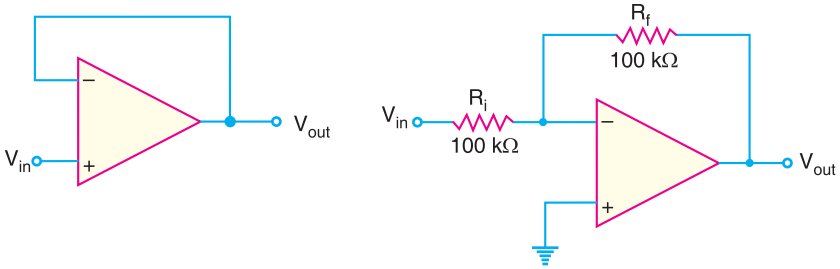


Fig. 25.104

12. Determine the approximate values of (*i*) I_{in} (*ii*) I_f (*iii*) V_{out} (*iv*) closed-loop voltage gain for the circuit in Fig. 25.105. **[(*i*) 455 μ*A* (*ii*) 455 μ*A* (*iii*) – 10*V* (*iv*) – 10]**

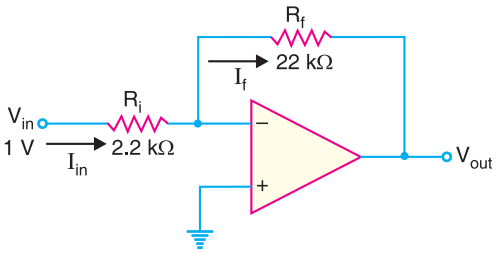


Fig. 25.105

13. Calculate the output voltage of the circuit in Fig. 25.106 for $R_f = 68$ kΩ. **[$V_o = -3.39$ V]**

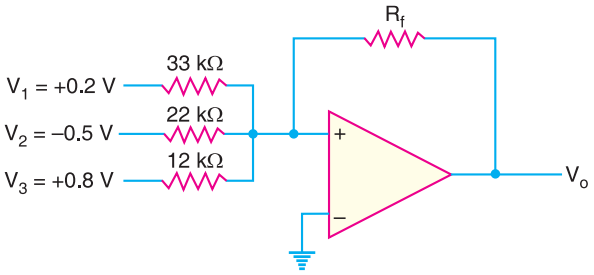


Fig. 25.106

14. What output voltage results in the circuit of Fig. 25.107 for $V_1 = +0.5$ V? **[$V_o = 0.5$ V]**

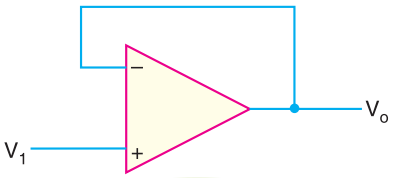


Fig. 25.107

15. Calculate the output voltages V_2 and V_3 in the circuit of Fig. 25.108. **[$V_2 = -2$ V ; $V_3 = 4.2$ V]**

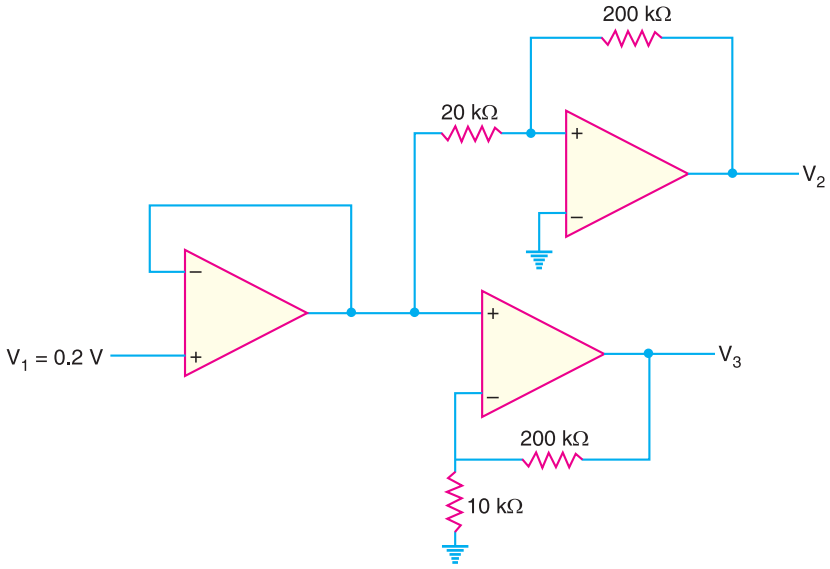


Fig. 25.108

Discussion Questions

1. What is the difference between a discrete circuit and an integrated circuit (IC)?
2. Why are OP-amps produced as IC?
3. What is the difference between differential amplifier and the conventional amplifier?
4. What do + and – signs on the symbol of an OP-amp indicate?
5. Why is OP-amp generally operated with negative feedback?
6. Why is common-mode gain of a DA very low?
7. What is the importance of CMRR?
8. When is OP-amp driven to saturation?
9. In which circuit we take the advantage of high open-loop voltage gain of an OP-amp?
10. What is a noninverting amplifier?
11. Why is the input impedance of an OP-amp very high?
12. Why is the open-loop voltage gain of an OP-amp high?
13. What do you mean by virtual ground?
14. Why is the output impedance of an OP-amp very low?
15. What are the advantages of negative feedback in OP-amps?

Top