

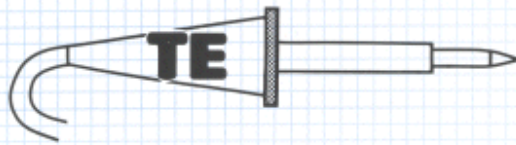
A TALKING ELECTRONICS PTY LTD
PUBLICATION

DIGITAL ELECTRONICS

REVEALED

by

Colin Mitchell



DIGITAL ELECTRONICS REVEALED



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Introduction

This book is a compilation of the 10 MINUTE DIGITAL COURSE from TALKING ELECTRONICS, Issues 1 to 14.

It is the result of numerous requests from readers and teachers asking for the digital pages to be collected as a single reference source.

You can approach this book in two ways. It can be read as a novel, from cover to cover, or used as a textbook for quick referencing.

Either way you will find a lot of information has been packed into a small space.

The magic of this book is it provides the maximum of detail with the minimum of reading. It presents everything in an easy-to-grasp way.

The layout is based on a "blackboard" method of learning. Surprisingly, we grasp a subject more easily when it is presented in hand-written form. Possibly a throwback to our early years of schooling when everything was presented on a blackboard and from that time we accept this type of format as FACTUAL.

Seeing this format in book-form has a double impact. Not only do we want to see what has been presented but we are constantly mystified as to why the information didn't go to the typesetters.

When you realise it takes 3 times longer to hand write a page, you will understand why it is rarely done.

On the other hand, it allows freedom for presentation of sketches and ideas that can save a thousand words.

If this is your first introduction to grid pages, you will find the supporting articles in TALKING ELECTRONICS magazine very helpful. TE is designed to increase your knowledge of digital circuits through construction and experimentation. I hope you can find someone with some of the old issues as most of them have sold out and we cannot supply them any more. Due to the enormous demand for the earlier issues, some of them are being reprinted and released through Dick Smith stores. Don't ring us, wait to see them in the stores. They are all a valuable addition to your library so don't miss a single issue when you find them as they may never be released again.

If you are a student, show this publication to your friends and teachers. Many already know about us but you may find a newcomer who has just started to get interested in electronics. But be warned, don't lend him your copy as you will never get it back!

If you are undertaking an electronics course, ask your teacher to buy a class set so you can have a copy at home as well as one at school. This way we sell lots more copies.

No matter what level of electronics you are taking, I know you will find the information invaluable.

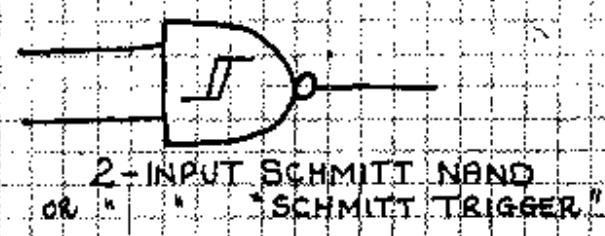
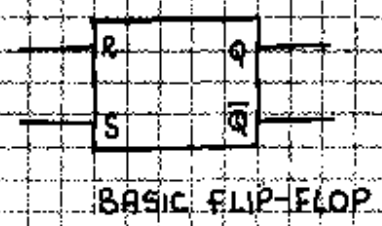
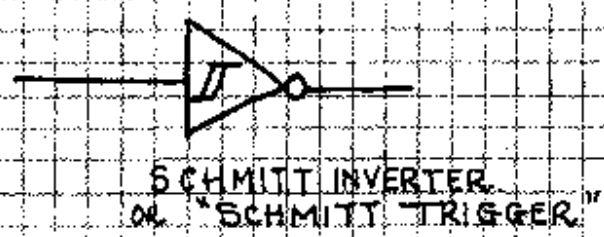
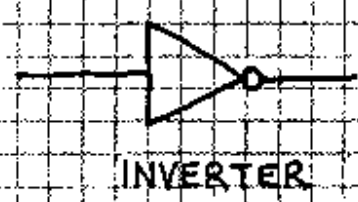
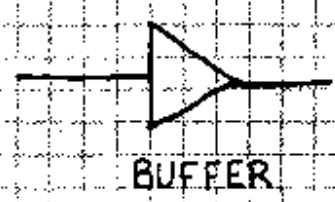
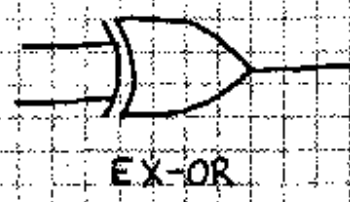
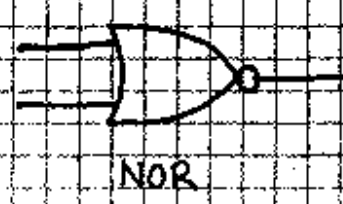
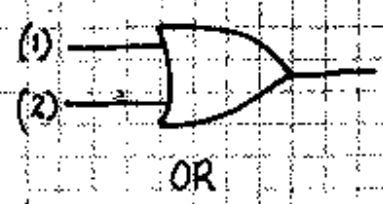
Keep it handy and see how crumpled it gets over the next few years!

All the best,

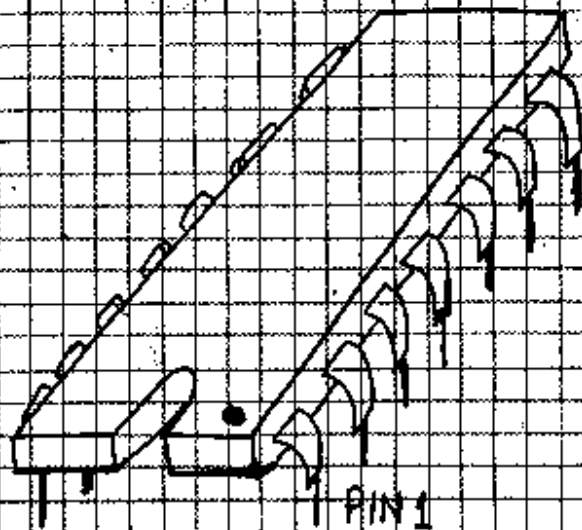
Colin Mitchell.

September 1983 & August 1993

**THESE ARE THE LOGIC SYMBOLS
USED IN THIS COURSE**



Π = SCHMITT SYMBOL
OR "HYSTERESIS" SYMBOL



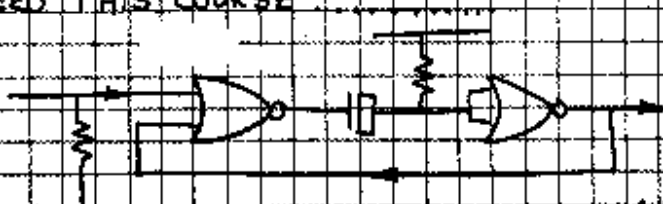
THIS IS AN INTEGRATED CIRCUIT OR "CHIP" OR MORE COMMONLY CALLED AN "IC". INSIDE THEY CONTAIN FROM A DOZEN TRANSISTORS TO MANY THOUSANDS OF TRANSISTORS. BUT THE WAY IN WHICH THESE IC'S OPERATE IS QUITE UNLIKE A TRANSISTOR... THEY OPERATE MORE LIKE SWITCHES & RELAYS. BECAUSE THEY ARE DIFFERENT WE MUST STUDY THEM IN A NEW LIGHT. THEY ARE THE ELEMENTS OF OUR NEW ELECTRONIC AGE... THE BUILDING BLOCKS OF THE FUTURE AND TO UNDERSTAND THEM WILL OPEN THE GATE-WAY TO

DIGITAL ELECTRONICS

DIGITAL ELECTRONICS DEALS WITH TWO VERY SIMPLE CONDITIONS. ALL THE CIRCUITS ARE DESIGNED TO GIVE AN OUTPUT WITH ONE OF TWO VALUES. THEY ARE EITHER ON OR OFF. NOTHING COULD BE SIMPLER AND NOTHING COULD BE MORE ACCURATE. IN FACT THE CIRCUITS ARE SIMPLE AND THE SCIENCE IS EXACT. THE ONLY PROBLEM IS IN CO-ORDINATING A NUMBER OF INPUTS TO GIVE US AN OUTPUT. AND THIS IS WHERE DESIGN COMES IN. YOU MAY HAVE 7 INPUTS TO BE FED TO ONE OUTPUT AND 6 OF THESE INPUTS MUST BE ON. HOW WOULD YOU DO IT? ANOTHER SITUATION MAY INVOLVE COUNTING. HOW WOULD YOU DESIGN A CIRCUIT TO COUNT TO 200, THEN RESET. IT'S SIMPLE WITH DIGITAL ELECTRONICS. SINCE EACH CIRCUIT HAS ONLY AN ON-OFF CONDITION IT CAN ONLY COUNT TO 2. THIS MEANS YOU WILL NEED LOTS OF SIMPLE CIRCUITS TO COUNT TO 200. SO BASICALLY DIGITAL ELECTRONICS CONSISTS OF MANY MANY MANY SIMPLE SIMPLE CIRCUITS.

Should I do this course? - WHAT WILL I LEARN?

IF YOU CAN DESCRIBE THE OPERATION OF THIS CIRCUIT, YOU DON'T NEED THIS COURSE

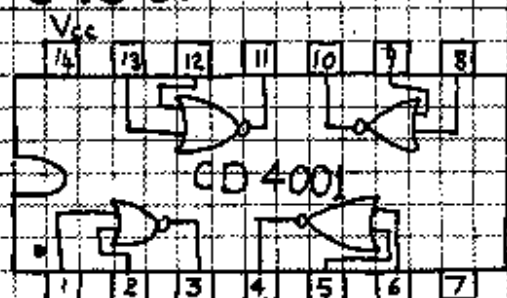


IF YOU CAN'T READ ON

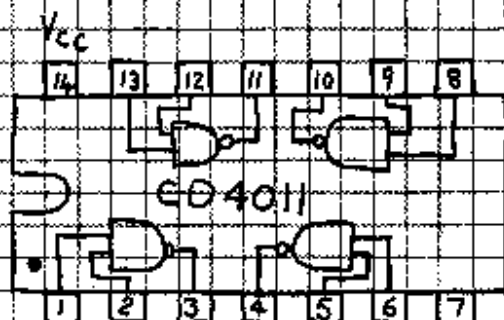
2 EVEN THOUGH DIGITAL ELECTRONICS PERFORMS 2 FUNCTIONS THESE 2 CONDITIONS CAN BE PACKAGED IN SO MANY DIFFERENT WAYS THAT WE CAN DESIGN THOUSANDS OF DIFFERENT IC'S. OBVIOUSLY THIS VARIETY WOULD BE TOO MUCH FOR US TO COVER. HERE SO WE WILL LIMIT OUR DISCUSSION TO 4 OR 5 VERY SIMPLE IC'S SUCH AS CD 4071, CD 4081, CD 4001 & CD 4011 AND MAYBE A FEW OTHERS.

THESE ARE ALL CMOS IC'S WHICH STANDS FOR COMPLEMENTARY - METAL - OXIDE - SILICON. THEY ARE THE BEST TYPE OF IC FOR EXPERIMENTAL PROJECTS AS THEY CAN WITHSTAND WIDE VARIATIONS IN SUPPLY VOLTAGE AND CONSUME VERY LITTLE CURRENT MAKING THEM IDEAL FOR BATTERY OPERATED EQUIPMENT. THE ONLY WEAKNESS WITH CMOS IC'S IS ITS SUSCEPTABILITY TO STATIC ELECTRICITY ENTERING THE INPUT PINS WHEN IT IS REMOVED FROM ITS PROTECTIVE WRAPPER. ONCE IT IS SOLDERED INTO A CIRCUIT, IT BECOMES QUITE ROBUST.

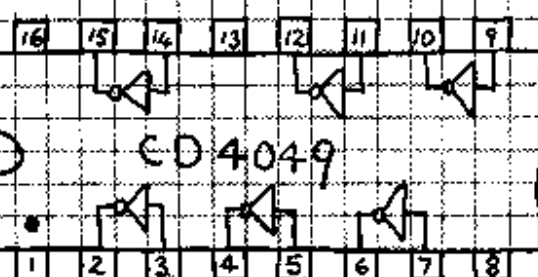
Our 6 IC's:



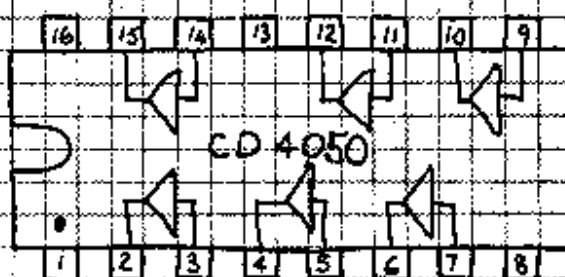
QUAD NOR-GATE



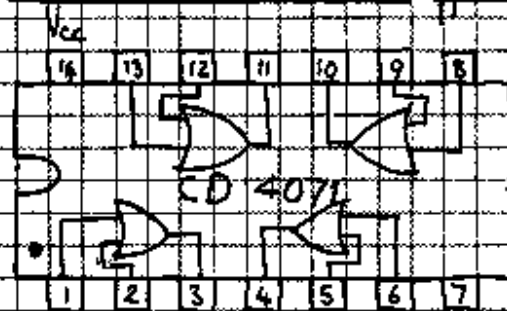
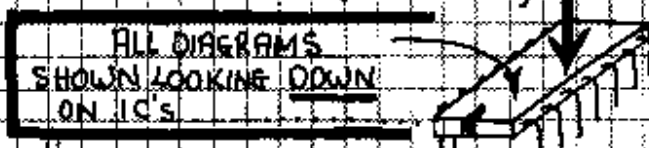
QUAD NAND GATE



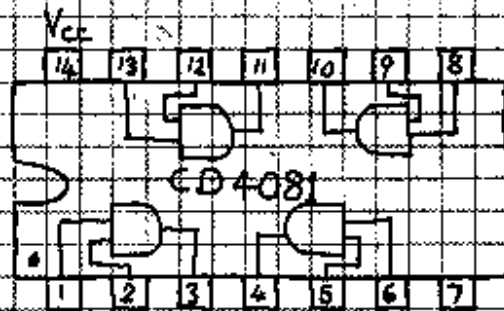
HEX BUFFER (INVERTING)



HEX BUFFER (NON-INVERTING)



QUAD OR GATE



QUAD AND GATE

3 SIMPLE GATES

OUR 6 IC'S IN BLOCK 2 ARE SIMPLE GATES. EACH IC CONTAINS ONE TYPE OF GATE. THEY FILL THE PACKAGE UNTIL ALL THE PINS ARE USED. THIS MEANS THEY CAN FIT 4-6 GATES IN AN IC.

FINDING PIN 1

ALL INTEGRATED CIRCUITS HAVE AN EQUAL NUMBER OF PINS DOWN EACH SIDE AND THEY ARE ALL EVENLY SPACED. IN OTHER WORDS THE CHIP IS NOT "POLARIZED". IT CAN BE PUT INTO CIRCUIT THE CORRECT WAY AROUND OR "AROUND THE WRONG WAY". IF YOU MAKE A MISTAKE THE CHIP WILL BE DAMAGED. THE ONLY WAY TO PREVENT THIS IS TO TAKE CARE & LOOK FOR THE IDENTIFICATION MARK(S)



UNFORTUNATELY THESE ARE A VERY POOR WAY OF IDENTIFYING PIN 1 AND A GREAT DEAL OF CARE MUST BE TAKEN WHENEVER AN IC IS INSERTED. DO NOT REFERENCE OFF ANY OTHER MARKS OR HOLES ON THE IC OR EVEN THE NUMBERING ON THE IC AS THESE MAY BE UP-SIDE-DOWN.

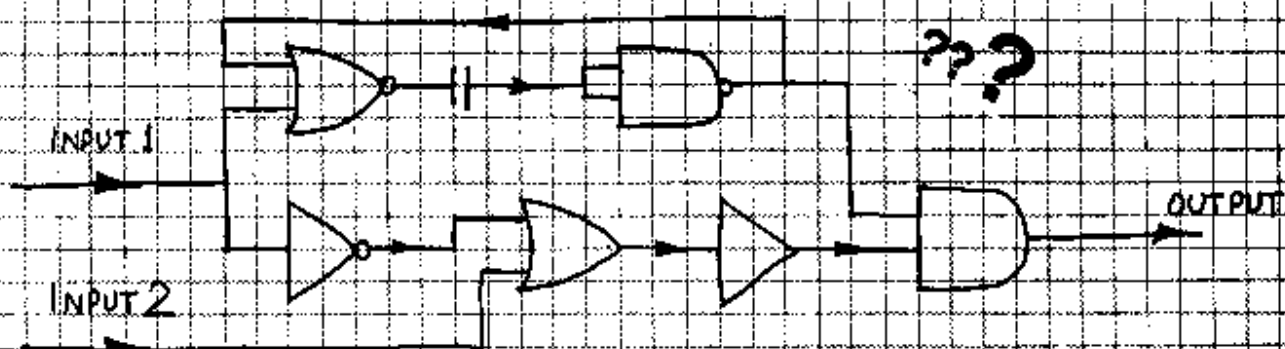
BUILDING BLOCKS

ALL ELECTRONIC DEVICES & CIRCUITS CAN BE DI-SECTED INTO BUILDING BLOCKS. IT MAKES UNDERSTANDING EASIER. IF YOU LEARN THE CHARACTERISTICS OF A NUMBER OF BLOCKS YOU CAN PIECE THESE FACTS TOGETHER TO CREATE A COMPLEX CIRCUIT. A GATE IS A BUILDING BLOCK.

OUR 6 SIMPLE GATES ARE:

AND = CD4081
OR = CD4071
BUFFER = CD4010
NAND = CD4011
NOR = CD4001
INVERTER = CD4009

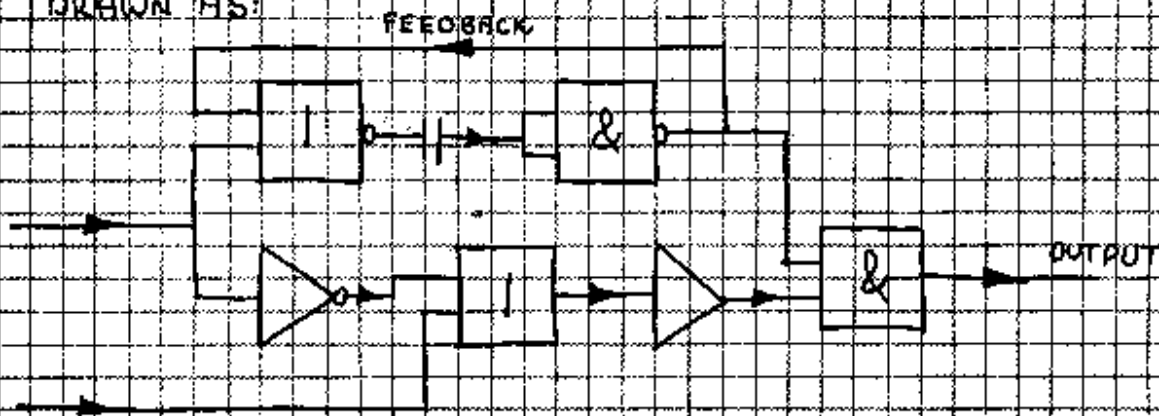
HERE IS A SIMPLE CIRCUIT USING THE 6 GATES. DOES IT WORK?



... READ ON AND FIND OUT

4 THE CIRCUIT IS A DIGITAL CIRCUIT (AND NOT AN AUDIO CIRCUIT) IT DOES NOT AMPLIFY. THE OUTPUT IS EITHER ON OR OFF & THE SIGNALS WITHIN THE CIRCUIT ARE ALSO ON OR OFF. THEY ARE NEVER HALF-ON OR HALF-OFF. THE ARROWS SHOW THE DIRECTION OF THE SIGNALS. THE NORMAL OR FORWARD DIRECTION IS \longrightarrow FEEDBACK PATHS ARE: \longleftarrow

THERE ARE TWO CONVENTIONS FOR SHOWING GATES. WE PREFER THE AMERICAN MIL-SPEC STYLE BUT THE SAA STYLE IS ALSO BEING TAUGHT DURING THE FIRST PART OF THIS COURSE. BOTH SCHEMATICS WILL BE SHOWN. UNDER THE SAA NOTATION THE PREVIOUS CIRCUIT WILL BE DRAWN AS:



THE STYLE OF REPRESENTING GATES WILL BE UP TO YOU. ONE SYSTEM IS FAR EASIER & QUICKER TO VISUALISE.

How do gates work?

TO UNDERSTAND HOW GATES WORK YOU DON'T HAVE TO KNOW ABOUT TRANSISTOR OPERATION OR ELECTRON FLOW. IN FACT YOU DON'T EVEN NEED TO KNOW HOW GATES ARE CONSTRUCTED. FOR OUR PRELIMINARY DISCUSSION, GATES CAN BE CONSIDERED AS SWITCHES. ALL YOU NEED TO KNOW IS THE VOLTAGE LEVELS AT WHICH THE INPUT GATES CHANGE STATE FROM HIGH-TO-LOW OR LOW-TO-HIGH.

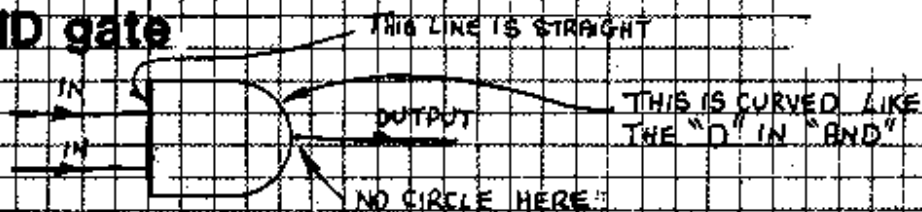
THE INPUT LINE TO ALL TYPES OF GATES IS DESIGNED TO DETECT ONLY 2 STATES: HIGH ... LOW

THE OUTPUT IS DESIGNED TO GIVE ONLY TWO STATES ALSO: HIGH ... LOW

THERE ARE NO VALUES SUCH AS HALF OR QUARTER OR "PARTLY ON". THIS MAKES THE OPERATION OF A DIGITAL CIRCUIT EXTREMELY ACCURATE.

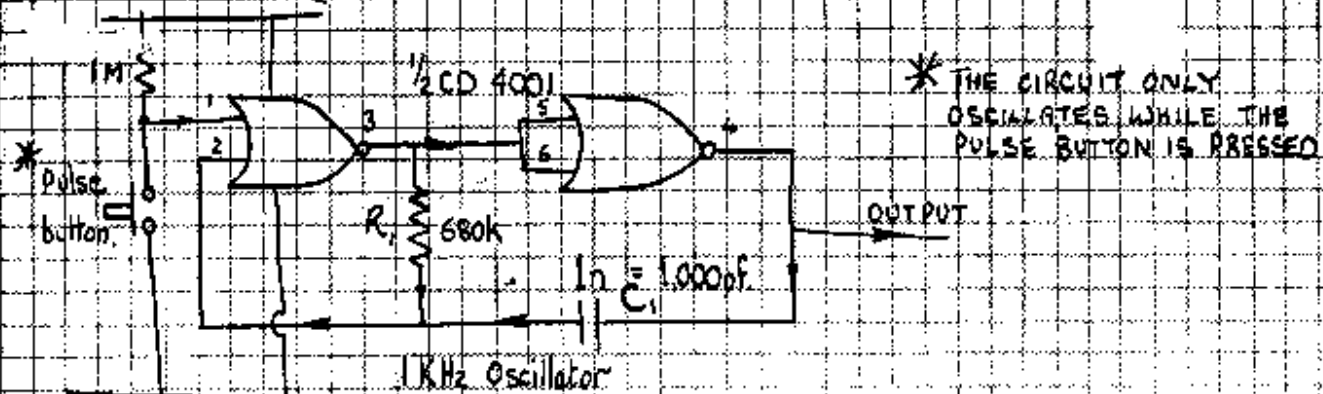
Looking at gates

1. The AND gate



22 MULTIVIBRATORS:

THE MOST USEFUL MULTIVIBRATOR IS THE ASTABLE OR SQUARE-WAVE GENERATOR. THE CIRCUIT SHOWS $\frac{1}{2}$ CD 4001 IC USED TO MAKE A 1KHz ASTABLE MULTIVIBRATOR.

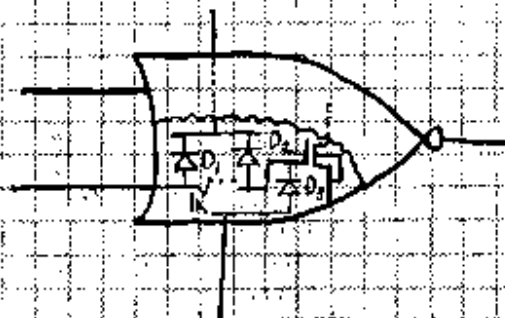


HOW THE CIRCUIT WORKS:

THE CIRCUIT IS SHOWN GATED OFF DUE TO PIN 1 BEING BIASED HIGH VIA THE UPPER 1M RESISTOR. [A HIGH ON EITHER INPUT GATE WILL CAUSE THE OUTPUT TO GO LOW] THUS PINS 3, 5 & 6 ARE LOW. PINS 5 & 6 ARE THE INPUT GATES OF THE SECOND NOR GATE AND WILL CAUSE THE OUTPUT PIN 4 TO BE IN A HIGH STATE UNTIL PIN 1 GOES LOW MOMENTARILY.

WHEN A PULSE OF SHORT DURATION IS DETECTED ON PIN 1 IT WILL CAUSE PIN 3 TO GO HIGH AND THE OUTPUT PIN 4 TO GO LOW. SEE TRUTH TABLE FOR NOR GATES TO VERIFY THIS. CAPACITOR C, BEING FULLY CHARGED WILL ATTEMPT TO MAKE PIN 2 SWING NEGATIVE WITH RESPECT TO THE 0V RAIL. LET ME EXPLAIN THIS IN ANOTHER WAY WHICH MAY BE EASIER TO UNDERSTAND. SUPPOSE WE CONSIDER THE CAPACITOR TO BE A 9V RECHARGEABLE BATTERY INITIALLY THE BATTERY IS IN A STATE OF FULL CHARGE. WHEN A TRIGGER PULSE IS RECEIVED AT PIN 1 THE FIRST NOR GATE WILL GO HIGH AND SINCE IT IS DIRECTLY COUPLED TO THE SECOND NOR GATE IT CAUSES THE OUTPUT PIN 4 TO GO TO 0V. THIS IS EQUIVALENT TO UNPLUGGING THE FULLY CHARGED BATTERY AND PLACING ITS POSITIVE TERMINAL ON THE 0V RAIL.

IN BUILT INTO EACH GATE OF THE IC ARE 3 DIODES, ONE OF WHICH PREVENTS THE INPUT SIGNAL GOING BELOW 0V (THE OTHER TWO ARE DISCUSSED LATER). SO WHEN THIS -9V IS PRESENTED AT INPUT GATE 2, DIODE D_2 CONDUCTS VIA THE 1K RESISTOR AND QUICKLY REMOVES THE CHARGE ON THE CAPACITOR (OR BATTERY ANALOGY). WITH THE CAPACITOR FULLY DISCHARGED, IT BEGINS TO RECHARGE IN THE REVERSE DIRECTION FROM THE HIGH ON PIN 3 VIA R, AND THE VOLTAGE ON PIN 2 STARTS TO RISE EXPONENTIALLY TOWARDS THE POSITIVE RAIL. DURING THIS RISE THE THRESHOLD VOLTAGE IS ATTAINED AND CAUSES THE OUTPUT PIN 3 TO GO LOW AND PIN 4 TO GO HIGH.

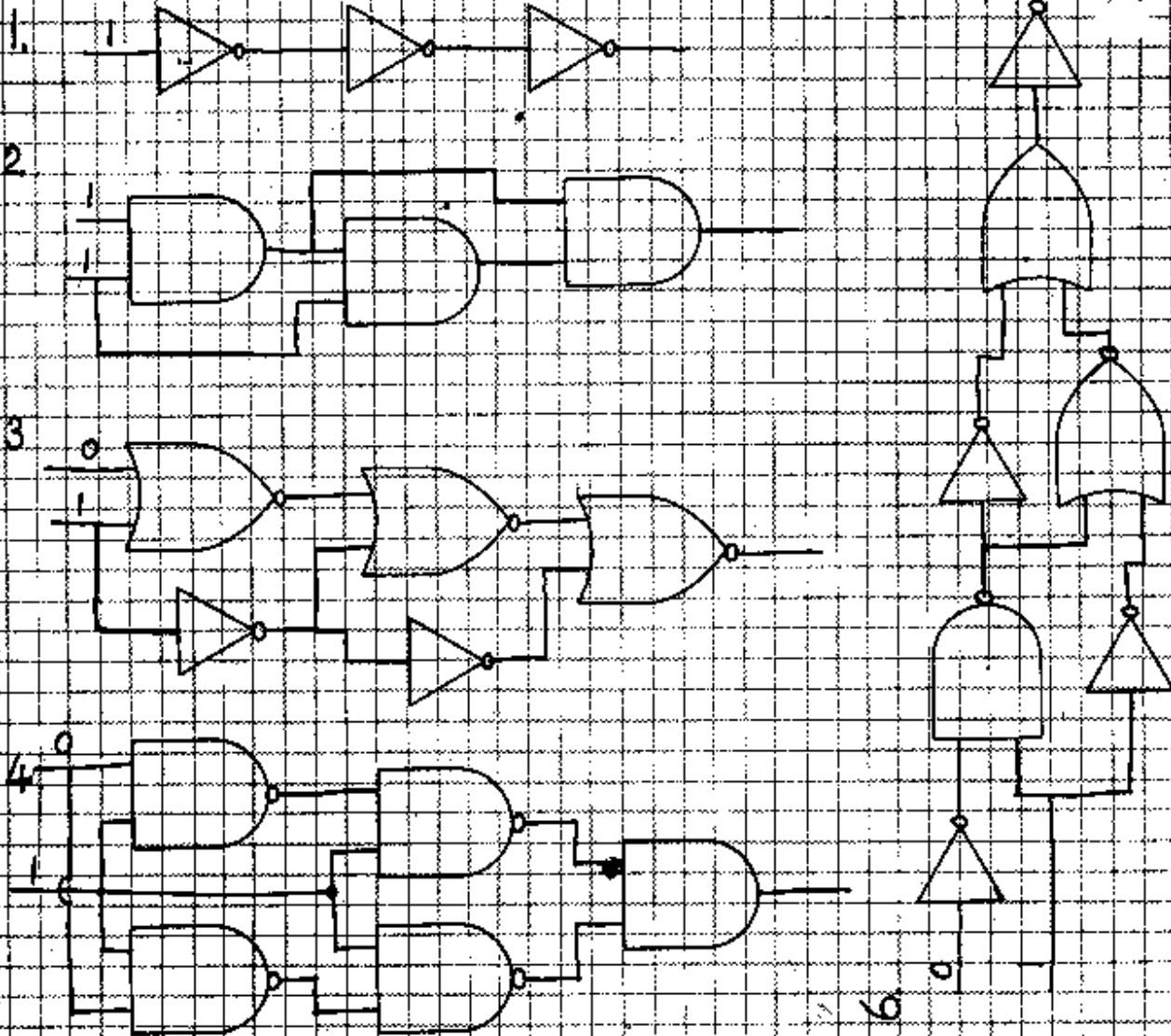


PARTLY BROKEN AWAY SECTION SHOWING THE 3 INPUT PROTECTION DIODES CONNECTED TO EACH GATE.

26

GATE QUIZ

USING BLOCKS 8, 9, 10, 14 & 15 TEST YOUR ABILITY TO TRACE OUT GATE CIRCUITS THE HIGH OR LOW APPEARS SIMULTANEOUSLY AT THE INPUTS AS SHOWN DETERMINE THE OUTPUT OF EACH OF THESE ARRANGEMENTS:



5. (a) DRAW 2 NAND GATES AND WIRE THEM TO FORM AN AND GATE.

(b) DRAW 2 NOR GATES AND WIRE THEM TO FORM AN OR GATE.

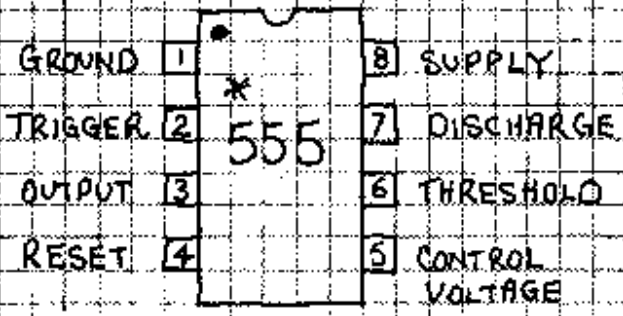
(c) HOW DO YOU CONNECT A NOR GATE TO FORM A NOT FUNCTION?

09 07 06 12 07

47

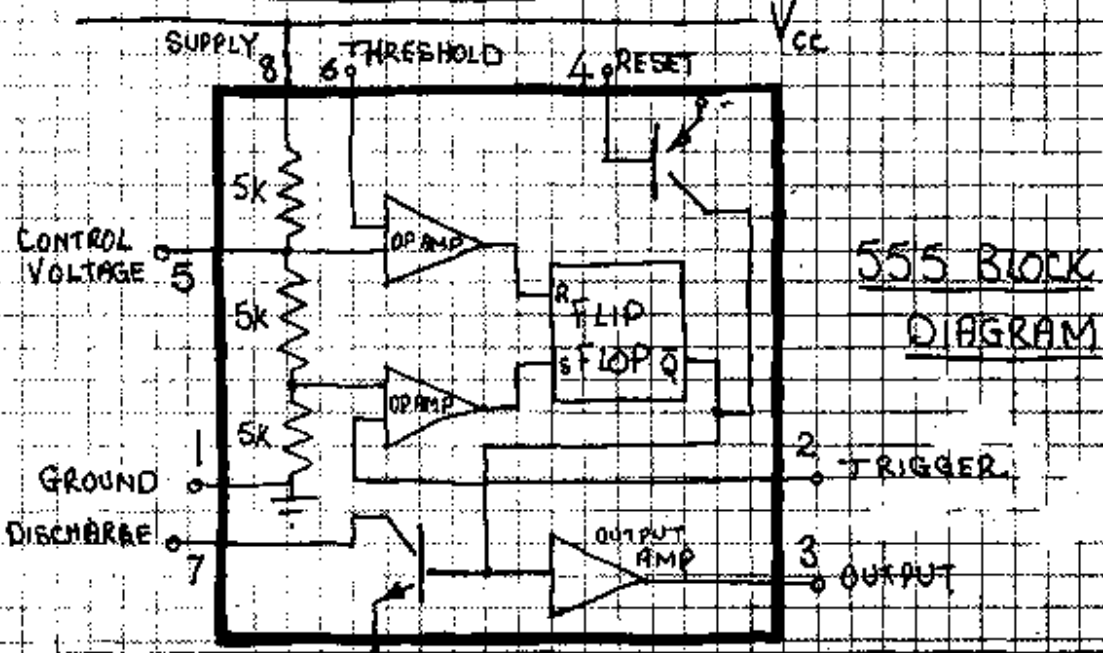
The 555

OUR FIRST DEDICATED IC IN THIS SERIES IS A 555 (PRONOUNCED "TRIPLE FIVE") THIS IS A SHORT-FORM WAY OF SAYING LM555 OR SE 555 OR NE 555. IT IS SPECIALLY DESIGNED TO OPERATE AS A MULTIVIBRATOR WHICH CAN TIME FROM MICRO-SECONDS TO SEVERAL HOURS. IT IS A TTL DEVICE AND AS SUCH IS NOT PRONE TO STATIC ELECTRICITY BUT ITS POWER CONSUMPTION IS CONSIDERABLY MORE THAN CMOS IC'S AND MUST BE TAKEN INTO ACCOUNT WHEN DESIGNING FOR BATTERY OPERATION. THE 555 TAKES 10mA FROM THE SUPPLY WHEN THE OUTPUT IS HIGH AND 1mA WHEN THE OUTPUT IS LOW. WHEN OPERATING AS AN OSCILLATOR WE CAN CONSIDER THE POWER CONSUMED TO BE EQUAL TO THAT OF A LED. A CMOS VERSION HAS BEEN INTRODUCED WITH THE PART NUMBER LM 7555 BUT AS YET IS CONSIDERABLY MORE EXPENSIVE THAN THE 555. WHEN THE PRICE FALLS IT WILL BE A VERY GOOD CHOICE AS IT CONSUMES ONLY 20µA. TO DATE IT DOES HAVE A NUMBER OF LIMITATIONS SUCH AS OUTPUT CURRENT CAPABILITY & MAXIMUM VOLTAGE LEVELS ON THE TRIGGERING PINS BUT THESE MAY BE OVERCOME IN LATER VERSIONS.



* MAY BE:
 LM 555
 NE 555
 SE 555

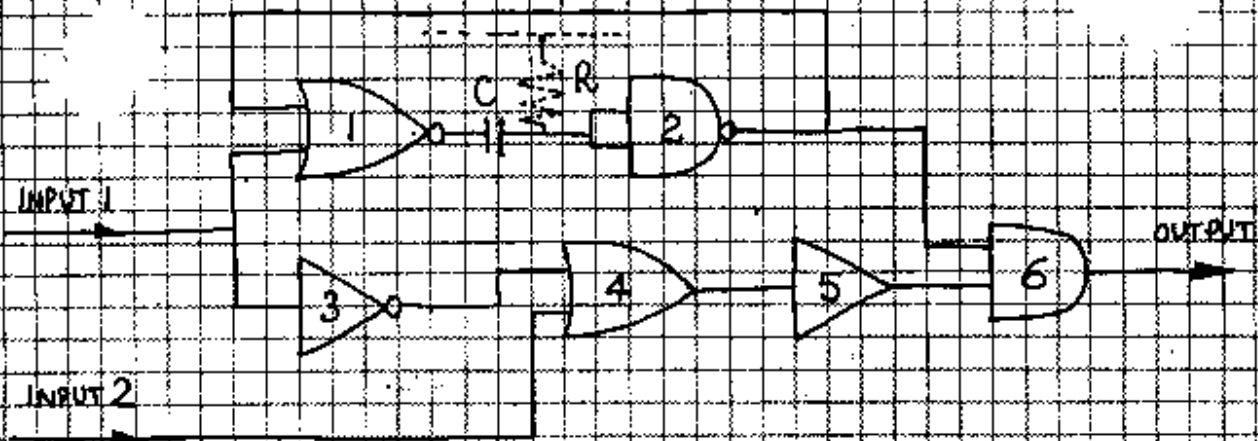
555 PIN OUTS



555 BLOCK DIAGRAM

What have you learnt?

IN BLOCK 3 WE ASKED IF THIS CIRCUIT WOULD WORK:



BY NOW YOU SHOULD BE ABLE TO LOCATE THE ONE FAULT IN THE CIRCUIT. GATE 2 NEEDS A PULL-UP RESISTOR TO COMPLETE THE DELAY CIRCUIT COMPRISING GATES 1 & 2.

FOLLOW THROUGH THIS DISCUSSION AND FILL IN THE BLANKS:

INITIALLY INPUTS 1 & 2 ARE LOW. TO DETERMINE THE STATE OF GATE 1 WE MUST KNOW THE LOGIC LEVELS ON BOTH ITS INPUTS. THUS WE NEED TO LOOK AT GATE 2 WHICH IS SUPPLYING THE FEEDBACK PULSE TO GATE 1. BOTH INPUTS OF GATE 2 MUST BE (1) MAKING THE OUTPUT LOW. THIS IS FED BACK TO GATE 1 TO CREATE A (2) OUTPUT. THE OUTPUT OF GATE 3 WILL BE (3). THE OUTPUT OF 4 WILL BE (4). THE OUTPUT OF 5 WILL BE (5) AND THE OUTPUT OF 6 WILL BE (6).

WHEN INPUT 1 GOES HIGH, THE OUTPUT OF GATE 1 WILL GO (7) ALLOWING THE UNCHARGED CAPACITOR TO BRING DOWN THE INPUTS OF GATE 2 AND CHANGE THE OUTPUT TO A (8). THIS WILL BE TRANSFERRED BACK TO GATE 1 AND TAKE OVER FROM THE INPUT.

MEANWHILE GATE 3 OUTPUT WILL CHANGE FROM (9) TO (10).

GATE 4 OUTPUT WILL CHANGE FROM (11) TO (12).

GATE 5 FROM (13) TO (14).

GATE 6 FROM (15) TO (16).

WHEN INPUT 1 GOES LOW IT WILL HAVE ANY OR NO EFFECT ON GATE 1.

GATES 3, 4 & 5 WILL OR WILL NOT CHANGE.

GATE 6 WILL CHANGE FROM (17) TO (18).

AFTER A PERIOD OF TIME THE INPUT TO GATE 2 WILL RISE ABOVE LOW LEVEL AND CHANGE THE OUTPUT FROM (19) TO (20).

GATE 6 WILL CHANGE FROM (21) TO (22).


INPUT 2 WILL HAVE AN EFFECT ON GATE 6 WHEN GATE 2 IS (23).

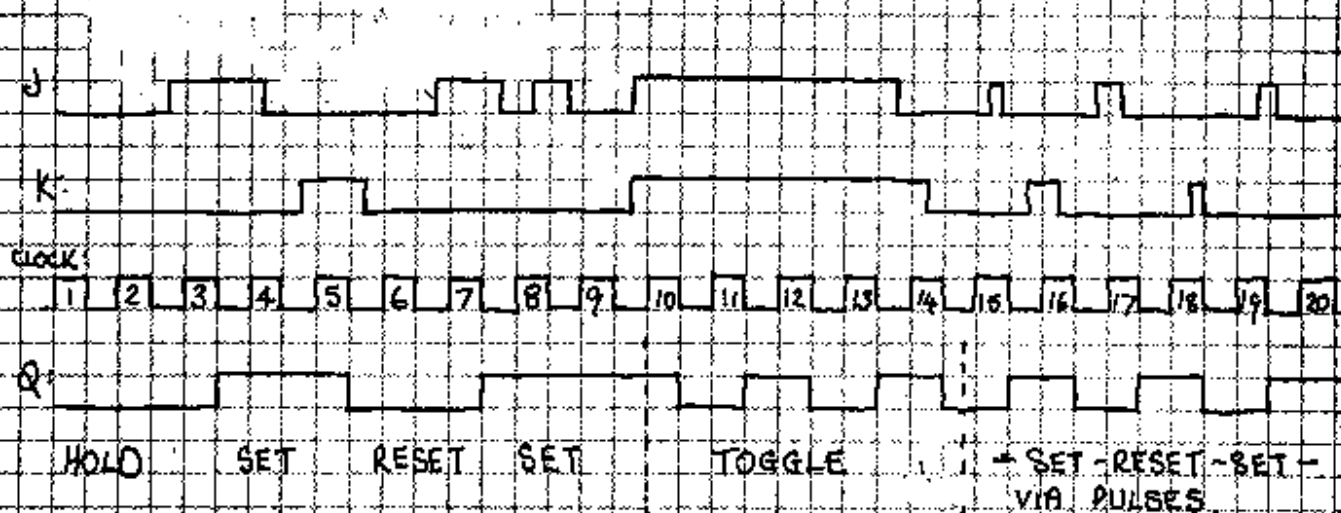
(1) HIGH (2) HIGH (3) HIGH (4) HIGH (5) HIGH (6) LOW (7) LOW (8) HIGH (9) HIGH (10) LOW

(11) HIGH (12) LOW (13) HIGH (14) LOW (15) LOW (16) LOW (17) NO (18) WILL (19) LOW

(20) HIGH (21) HIGH (22) LOW (23) HIGH (24) LOW (25) HIGH & INPUT 1 IS HIGH.

THE 4 MODES OF OPERATION OF A J-K FLIP FLOP CAN BE PRESENTED ON A SINGLE TIMING DIAGRAM. THESE WAVEFORMS APPLY TO A NEGATIVE-EDGE TRIGGERED MASTER-SLAVE FLIP FLOP.

CLOCK 



INTERPRETING THE TIMING DIAGRAM:

THE OUTPUT OF THE FLIP FLOP IS INITIALLY LOW. CLOCK PULSES 1 & 2 HAVE NO EFFECT AS BOTH J & K LINES ARE LOW & THE FLIP FLOP IS INHIBITED. - IT IS IN THE FREEZE OR HOLD MODE.

WHEN THE J INPUT GOES HIGH, THE RISING EDGE OF THE CLOCK "SETS" THE MASTER SECTION OF THE FLIP FLOP. DURING CLOCK PULSE 3. WHEN THIS CLOCK PULSE FALLS, IT IS THE FALLING EDGE OR NEGATIVE EDGE WHICH CAUSES THE FLIP FLOP TO PASS THE CONTENTS OF THE MASTER TO THE SLAVE LATCH & THIS IS WHEN WE SEE THE RESULT ON THE OUTPUT Q.

CLOCK PULSE 4 SEES A J INPUT FOR A PORTION OF THE TIME THE INPUTS ARE OPEN AND THIS IS SUFFICIENT TO KEEP A "SET" CONDITION.

CLOCK PULSE 5 SEES THE J & K INPUTS IN THE RESET MODE AND ON THE TRAILING EDGE OF PULSE 5 THE Q OUTPUT IS RESET. CLOCK PULSE 6 SEES THE INPUTS IN THE HOLD MODE & THE FLIP FLOP REMAINS RESET.

CLOCK PULSE 7 SETS THE FLIP FLOP (J=1, K=0) & CLOCK PULSE 8 SEES A SET CONDITION FOR PORTION OF THE CLOCK PULSE. CLOCK PULSE 9 SEES THE HOLD MODE & THE FLIP FLOP REMAINS SET.

CLOCK PULSE 10 SEES THE TOGGLE MODE WHERE BOTH INPUTS ARE HIGH. ON THE TRAILING EDGE OF PULSE 10 THE Q OUTPUT TOGGLES TO A LOGIC LOW LEVEL. CLOCK PULSES 11, 12 & 13 ARE ALSO TOGGLE CONDITIONS & THE OUTPUT CHANGES ITS STATE AFTER EACH PULSE.

CLOCK PULSE 14 SEES A RESET CONDITION, CLOCK PULSE 15 SEES A SET CONDITION EVEN THOUGH IT IS A SHORT PULSE, PULSES 16, 17, 18, 19 ARE ALL SHORT PULSES PRODUCING SET-RESET-SET CONDITIONS AT Q.

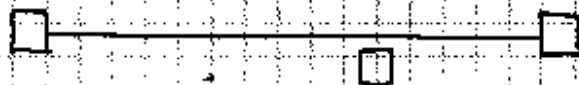
DEPENDING ON THE STATE OF THE INPUTS, THE OUTPUTS WILL PRODUCE 4 DIFFERENT EFFECTS:

1. FREEZE
2. REMAIN OR CHANGE TO SET CONDITION
3. " " " " " RESET CONDITION
4. TOGGLE

THE TOGGLE FEATURE CAN BE USED TO PRODUCE A DIVIDE-BY-2 STAGE AND THE FLIP FLOP CAN BE CASCADED TO PRODUCE LONG LINES OF DIVISION STAGES. THESE SOON BECOME EFFECTIVE. WITH 7 STAGES THE DIVISION IS 128 AND 12 STAGES PRODUCES A DIVIDE-BY-4096 COUNTER.

THIS IS THE TOPIC FOR THE NEXT SECTION

QUIZ:



1. WHEN A LATCH IS STORING A BINARY 1 IT IS IN THE _____ (SET, RESET) MODE.
2. DRAW THE BLOCK DIAGRAM FOR AN R-S FLIP FLOP.
3. IF A FLIP FLOP IS RESET THE Q OUTPUT IS _____ (HIGH, LOW).
4. THE NORMAL OUTPUT OF A FLIP FLOP IS Q, Q.
5. FOR AN ACTIVE LOW R-S FLIP FLOP, SUPPLYING THE R LINE WITH A _____ (HIGH, LOW) WILL (CLEAR, SET) THE Q OUTPUT TO A _____ (0, 1).
6. ASSUME AN R-S LATCH IS SET. A LOW TO THE S INPUT WILL:
 - (a) DO NOTHING
 - (b) CHANGE THE FLIP FLOP TO RESET
7. BOTH INPUTS OF A NOR LATCH ARE HIGH. THE STATE OF THE LATCH IS:
 - (a) SET
 - (b) RESET
 - (c) UNDESIRABLE OR PROHIBITED
 - (d) CAN'T TELL, NOT ENOUGH INFORMATION
8. WHEN THE NAND LATCH IS IN THE "LIMBO" CONDITION BOTH OUTPUTS WILL BE: _____ (HIGH, LOW).
9. Q & Q OUTPUTS SHOULD ALWAYS BE:
 - (a) THE SAME
 - (b) LOW
 - (c) HIGH
 - (d) COMPLEMENTARY
10. STATE 2 USES FOR A LATCH:
11. COMPLETE THIS DIAGRAM OF A NAND GATE LATCH.
12. A FLIP FLOP OPERATING IN STEP WITH A CLOCK IS SAID TO BE OPERATING:
 - (a) SYNCHRONOUSLY
 - (b) ASYNCHRONOUSLY
13. WHAT DOES "R-S" STAND FOR?