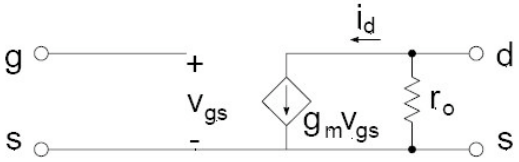
FET AMPLIFIERS (v5)

Safety: In this lab, voltages are less than 15 volts and this is not normally dangerous if you have dry skin. However, take extra care when you have a cut or break in the skin.

Objective: This lab is to learn how to design and implement FET amplifiers and learn the frequency response of real systems.

Preparation: Prior to the lab, **design** a FET amplifier (Figure 1) with a **voltage gain** $A_V = -5$. Design for $V_{DD} = 10$ V, $I_D = 5$ mA, $V_{DS} = 5$ V, and $R_{in} > 100$ kΩ. Assume $V_{GS} \approx 3$ V.

The following analysis is appropriate for good quality transistors where the output current I_D is largely independent of the output voltage V_{DS} (the output characteristic curves are approximately "flat"). We **calculate amplifier ac gain** using the small signal FET transconductance g_m and we assume r_o can be neglected because it is very large in comparison to other circuit resistances. The small signal FET equivalent circuit is shown in the following diagram.



$$e_{in} = V_{gs} + i_d R_S = \frac{i_d}{g_m} + i_d R_S$$

$$e_o = -i_d R_D$$

$$\frac{e_o}{e_{in}} = -\frac{R_D}{\frac{1}{g_m} + R_S}, \quad g_m \approx \frac{I_d}{100\,\text{mV}}$$

Where $\mathbf{g_m}$ is valid in exponential region

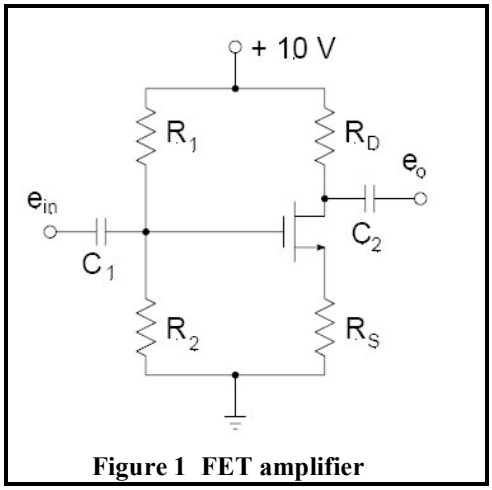


Figure 1 FET amplifier

The input resistance is essentially R_1 // R_2 and the output impedance is essentially equal to R_D if r_o is very large. Small signal ac gain is calculated assuming that capacitors have negligible impedance. See Appendix 1 on selecting appropriate capacitors. For $I_D = 5$ mA, g_m is approximately 50 mA/volt and $1/g_m$ is 20 ohms. This g_m approximation is valid in the sub-threshold region ($I_D < 10$ mA for IRFD110).

Procedure:

1. Construct the amplifier, using an IRFD110 FET and other components indicated in Figure 1. Use 250 kΩ variable resistor (potentiometer or decade box) for R_2, set to the calculated value before connected to the circuit. **Do not connect a signal generator and the capacitor C_1 to the input yet.** Adjust R_2 (if necessary) until I_D is approximately 5 mA. Once this has been accomplished, make note of the new value of R_2 and I_D, V_{DS}, V_G, and V_{GS}. You may now remove the ammeter (used to measure I_D) and any voltmeters. Connect capacitor C_1 and then

apply a small 1 kHz signal to **measure the ac voltage gain** of the circuit without load. If you have connected an oscilloscope channel directly to the drain of the FET, no coupling capacitor C_2 is required **provided that the scope is set to ac coupling**. Compare your measurements with your design values.

2. Devise a method to **measure the input impedance** of the amplifier at 1 kHz. Fully explain and document your methods in your lab book. Hint: you can use a decade resistor box and connect it in series to the input of the amplifier before the coupling capacitor. Monitor the signal amplitude after the decade box when you adjust the decade box values.

3. Place a **bypass capacitor, C_S = 470 µF**, in parallel with R_S. This capacitor will be **polarized**; ensure that the end with the band is connected to the most negative voltage. This bypass capacitance should have impedance much smaller (< 10%) than $1/g_m$ and the capacitor ac voltage should be very, very small. Verify this in your record keeping. Calculate the gain of the amplifier at 1 kHz and verify it experimentally. You will need to use the approximate value of g_m which you calculated using the drain current.

Optional Further Study:

Remove the bypass capacitor C_S added in part 3. Connect a 1 kΩ load resistor as shown in Figure 2. Determine the value of C_2 so that the load resistor/C_2 series combination has a lower cutoff frequency of 100 Hz. Will the input coupling capacitor, C_1, contribute a frequency-dependent response? How would you take this contribution into account?

Plot the log of the ac gain vs. log frequency for frequencies from 10 Hz to 5 MHz, and completely label it. For each decade of frequency, you need to take at least two ac gain measurements.

See Appendix 2 on measuring frequency response.

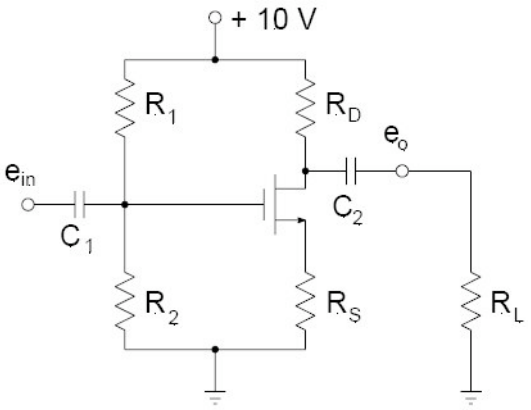


Figure 2 FET amplifier with load

Appendix 1 – selecting coupling capacitors:

Be careful when choosing your coupling capacitors (C_1 and C_2). For this experiment, our largest non-polarized capacitors may be used. Polarized capacitors tend to have "higher" capacitance values, usually ≥ 5 µF, and they are always marked with either a + or a – (or both) next to one of their terminals. They may also be marked with a band to indicate the negative end (same convention as a diode). Remember that the potential of the + terminal should be always higher than the – terminal when connected in a circuit. Otherwise, it will induce the leak current between the two terminals and eventually damage the capacitor. In the signal path of a circuit such as C_1 and C_2, this condition may not be met in all cases since the connected circuits are unknown. Therefore you should avoid polarized capacitors in the signal path.

Coupling capacitors must be chosen so that they have a "small" impedance at the frequency of interest compared with the input impedance of the circuit to which they're connected. This is to ensure that little voltage will be dropped or lost across the capacitor itself—after all, an amplifier is supposed to amplify voltages, not attenuate them. A good rule of thumb is that $Z_{coupling\ C}$ should be no more than approximately 10% of the input impedance of the amplifier (for the input coupling capacitor), or the input impedance of whatever circuit the amplifier drives (for the output coupling capacitor). For the FET amplifier you just constructed, the input impedance is supposed to be > 100 kΩ. Therefore the impedance of C_1 at the **lowest** frequency the amplifier is expected to see should be no more than approximately 10 kΩ. If this lowest frequency is expected to be 100 Hz, then $C_1 > 0.16$ μF. **For this experiment, select the appropriate coupling capacitors for C_1 at lowest frequency of 50 Hz.**

Similarly, the amplifier drives a load of 1 kΩ (Figure 2). Following the same argument the impedance of C_2 at the lowest expected frequency should be no more than approximately 100 Ω. If this lowest frequency is 100 Hz, then $C_2 > 16$ μF. If the largest non-polarized capacitors available are 2 μF, then C_2 would have to be made up of eight 2 μF capacitors in parallel. Alternately, a polarized capacitor could be used with appropriate care given to the polarity of the capacitor.

Appendix 2 – frequency response of the FET amplifier:

The typical Frequency Response of an amplifier is presented in a form of a graph that shows output amplitude (or, more often, voltage gain) plotted versus log frequency. Typical plot of the voltage gain is shown in Figure 3. The gain is null at zero frequency, then rises as frequency increases, level off for further increases in frequency, and then begins to drop again at high frequencies. The frequency response of an amplifier can be divided into three frequency regions.

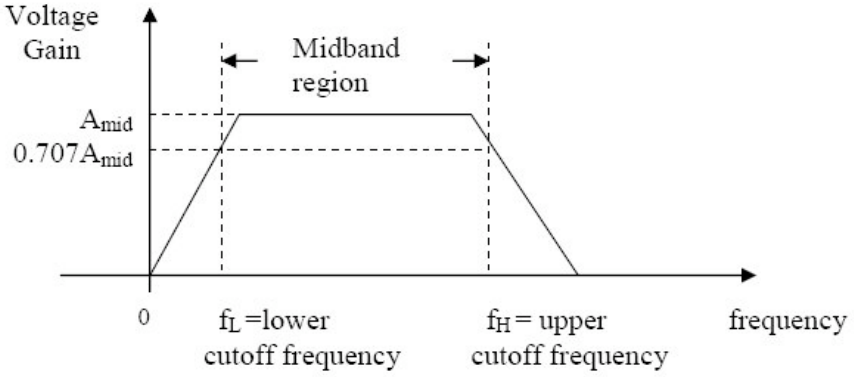


Figure 3: Diagram of voltage gain versus frequency for an amplifier.

The frequency response begins with the lower frequency region designated between 0 Hz and lower cutoff frequency. At lower cutoff frequency, f_L ,the gain is equal to 0.707 A_{mid}. A_{mid} is a constant midband gain obtained from the midband frequency region. The third, the upper frequency region covers frequency between upper cutoff frequency and above. Similarly, at upper cutoff frequency, f_H, the gain is equal to 0.707 A_{mid}. After the upper cutoff frequency, the gain decreases with frequency increases and dies off eventually.

The Lower Frequency Response:

Since the impedance of coupling capacitors increases as frequency decreases, the voltage gain of a FET amplifier decreases as frequency decreases. At very low frequencies, the capacitive reactance of the coupling capacitors may become large enough to drop some of the input voltage or output voltage. Also, the emitter-bypass capacitor may become large enough so that it no longer shorts the emitter resistor to ground. Approximately, the following equations can be used to determine the lower cutoff frequency of the amplifier, where the voltage gain drops 3 dB from its midband value (=0.707 times the midband A_{mid}):

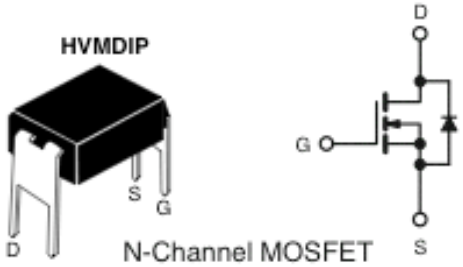
(1) $f_1 = 1/(2\pi r_{in} C_1)$ where:
f_1 = lower cutoff frequency due to C_1
C_1 = input coupling capacitance
r_{in} = input resistance of the amplifier

(2) $f_2 = 1/(2\pi r_{out} C_2)$ where:
f_2 = lower cutoff frequency due to C_2
C_2 = output coupling capacitance
r_{out} = output resistance of the amplifier

Provided that f_1 and f_2, are not close in value, the actual lower cutoff frequency is approximately equal to the largest of the two.

The Upper Frequency Response: - Transistors have inherent shunt capacitances between each pair of terminals. At high frequencies, these capacitances effectively short the ac signal voltage.

Appendix 3 – **IRFD110** Specifications: http://www.vishay.com/docs/91127/sihfd110.pdf



Third generation Power MOSFETs are designed to provide fast switching, ruggedized device design, and low on-resistance. The 4 pin DIP package is a low cost machine-insertable case which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W. Key specifications are in the following table.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	100	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V, T_J = 150 °C	-	-	250	µA
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 0.60 A[b]	-	-	0.54	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 0.60 A[b]	0.80	-	-	S
Continuous Source-Drain Diode Current	I_S		-	-	1.0	A
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz.	-	180	-	pF
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 5.6 A, V_{DS} = 80 V	-	-	8.3	nC
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 5.6 A,	-	6.9	-	ns
Turn-Off Delay Time	$t_{d(off)}$	R_g = 24 Ω, R_D = 8.4 Ω	-	15	-	