# THE EFFICIENCY OF A COUPLING CAPACITOR

**The efficiency of a coupling capacitor can be as low as 8% when a "class-A" stage is delivering energy to a low impedance load such as speaker.**
**Refer to the circuit on Page 2 of "The Transistor Amplifier" and section: "Designing an Output Stage. The circuit shows a "class-A" amplifier driving a speaker via a 100u electrolytic.**

**Now refer to the enclosed mathematical calculations.**

They develop the relationship needed to characterize an RC coupled common-emitter amplifier and the theoretical efficiency of the circuit referred to above. The same discussion can be modified for common-collector, common-base, as well as FET applications (as long as you're careful about certain boundaries, for example, ohmic mode in a JFET).

The development is as follows:

Equations 1 to 3 define the DC load line, which are all the possible steady-state currents and voltages for the collector-emitter (C-E) circuit. I use the lowercase "gamma" (the squiggly thing) to represent the so-called Q-point of the circuit, only so that I don't have to keep re-writing Vce / Vce(off). Gamma=0 means saturation, Gamma=1 means cutoff (no current).

The gain of semiconductors is very variable. DC beta can be all over the chart, and even a well-designed circuit will be impacted when beta changes (as when a device is replaced). But a well-designed circuit will employ stabilizing negative feedback in some way to stabilize the Q-point as much as possible.

Equations 4 and 5 describe the AC load line. The AC load line shows all the possible C-E circuit currents and voltages under a steady-state AC signal condition. The coupling capacitor is assumed to be very low in reactance compared to the circuit Thevenin impedance (Xc << Rth) at the frequency of interest. (I teach technicians to short coupling caps in their minds when analyzing most circuits of this type).

Why are we interested in the load lines? Well, the goal is to maximize efficiency - - and for a class A amplifier, that means we want the maximum undistorted output signal possible for a given Vcc (power supply) and RL (load) value. Because these load lines represent two sets of unknowns (with an overlap at the Q-point), a small amount of maths is needed to work with them to find the "sweet spot" where

maximum output can occur.

The Q-point of the circuit is the place where the AC and DC load line cross, and very importantly, it is the AC load line that determines the maximum peak-to-peak output AC voltage available from the collector circuit, known as the "compliance" of the circuit (Vpp). Equation 6 shows how we calculate Vpp. (You may be skeptical at this point that we can predict this, but we can!)

Please note that DC values are uppercase variables, and AC values (voltages and impedances) are lower case variables in this discussion. That's very important to know so that you don't pull your hair out trying to follow the line of reasoning.

Equation 6 is very important. It's shown as a pink sine-wave on the AC load line graph. I've broken Equation 6 into two parts below the AC load line graph. *The maximum peak-to-peak signal you can get is the sum of what the lower and upper parts of the AC load line can provide*. Furthermore, if the Q-point is in the wrong place, either the bottom or the top of the signal will be clipped first (saturation or cutoff clipping).

In other words, *a centered Q-point forces the two parts of Equation 6 to be equal!* (This is anti-intuitive to most technicians and engineers, who tend to be stuck thinking: "The best Q-point is halfway down the load line." That's not always correct!)

Equation 7 is just an extension of the thinking of Equation 6 - - that is, both halves of Equation 6 are equal when the Q-point is correctly located. But where, exactly, should that Q-point be? Oh yes, we need to "slide" the DC operating point to the right place. Remember Gamma, our abbreviation for Q-point? Substituting that into Equation 7a gives us Equation 8, which looks prettier as Equation 8a, but solved for Gamma (the Q-point), Equation 8b. (Equations 7 and 8 are not in any texts I'm aware of, but they're pretty self-evident.)

So now we know what Q-point to use. Let's put this to work in a less abstract context, an idealized class A common-emitter stage as shown on Page 2. I picked a voltage-divider biased circuit with a grounded emitter. (Whoa, you say, that isn't so smart! The Q-point will be unstable with this approach! You're right, with a grounded emitter, there's no DC negative feedback to stabilize the Q-point. If it makes you feel better, tie resistor R1 to the collector instead of Vcc. Feel better now?)

The point behind the idealized circuit is to develop the maximum efficiency possible. That's why the emitter is grounded. No AC or DC losses in the external portion of the emitter circuit this way!

Equation 1 chooses the collector resistor. For maximum efficiency, RC

must equal RL. That's the maximum power transfer theorem in action. I offer no proof of this here, but it can be shown with a little additional maths. (You can get more power out by lowering RC, but efficiency will really reduce. Likewise, you can increase RC to reduce current drain... but power delivered to the load will then fall greatly too, along with efficiency. You can't have your cake and eat it too!)

Equation 2 sets the DC Q-point. It turns out that Gamma needs to be 1/3 to get maximum output in this setup. (Again, Gamma=1/2 is a common misconception as the best Q-point... but that's clearly not the case here!)

Equation 2a calculates the maximum Vpp deliverable to the load. That turns out to be 2/3 of whatever Vcc you've chosen, given the conditions set up by Equations 1 and 2.

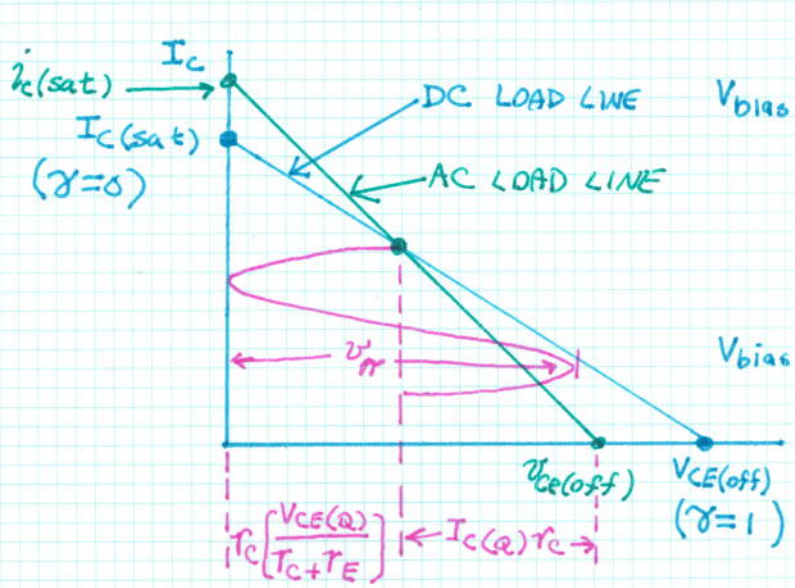
We're now almost there as far as efficiency goes. Equation 3 uses Ohm's law to get the maximum delivered power output. (P=V^2/R, or Vpp^2/8RL for a sinusoid). We now know the power output - - the hard part is done!

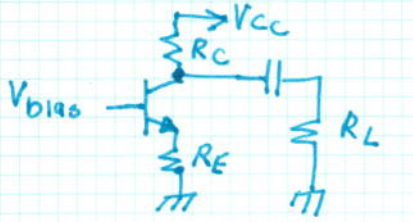
Equation 4 calculates power input. I've ignored the effect of any base-bias circuitry. That will lower efficiency further in a real circuit.

Equation 5 is the final efficiency calculation, $P_{out}/P_{in}$. Yes, it comes to 1/12, which is very poor indeed. (Of course, the transistor load line is actually a hyperbola, not a line, so your result will vary slightly - - and the circuit will most certainly be creating some distortion at this maximum level.)

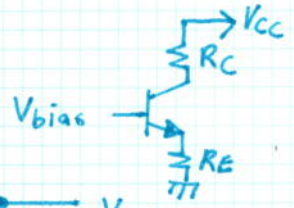
So can you practically demonstrate this? I bet so. The best Q-point is the bone of contention; add a pot to the base circuit so that you can sweep it up and down nicely while the thing is running. (Pots are necessary to test a circuit). Deliver a signal, drive it just beyond clipping, then adjust the pot for minimum distortion (or symmetric clipping). Reduce the signal, verify that clipping is symmetric. Then remove the signal and measure the collector DC voltage. You should see about 1/3 of the Vcc value, whatever that happens to be. While you're at it, measure the power taken from the supply and the load power to see if you get $8_{1/3}$ % (probably a little less depending on your base bias scheme). You will have demonstrated the practical design principle developed above.

Tom Wheeler




Composite




DC

CE BASIC RELATIONS
DE NØGSG
8-16-2012

**DC ANALYSIS**

(1) $I_{C(SAT)} = \dfrac{V_{CC}}{R_C+R_E}$ (3a) $I_{C(Q)} = \dfrac{V_{CC}(1-\gamma)}{R_C+R_E}$

(2) $V_{CE(OFF)} = V_{CC}$

(3) By definition, $\gamma = \dfrac{V_{CE}}{V_{CE(OFF)}}$ $0 \le \gamma \le 1$ Describes Q-point

**AC LOAD LINE**

(4) $i_{c(sat)} = I_{C(Q)} + \dfrac{V_{CE(Q)}}{r_C+r_E}$ AC saturation

(5) $v_{ce(off)} = V_{CE(Q)} + I_{C(Q)}(r_C+r_E)$ AC CUTOFF

**OUTPUT SIGNAL**

(6) $v_{pp} = r_C\left[\dfrac{V_{CE(Q)}}{r_C+r_E}\right] + I_{C(Q)}r_C$ OUTPUT COMPLIANCE

**DEFN - CENTERED 'Q'**

(7) $r_C\left[\dfrac{V_{CE(Q)}}{r_C+r_E}\right] = I_{C(Q)}r_C$

DEFINITION:
CENTERED AC Q-POINT
MEANS SYMMETRIC CLIPPING

(7a) $\dfrac{V_{CE(Q)}}{r_C+r_E} = I_{C(Q)}$

**HOW TO CENTER Q-POINT**

(8) $\dfrac{\gamma V_{CC}}{r_C+r_E} = \dfrac{V_{CC}(1-\gamma)}{R_C+R_E}$ ← EQ. 3a from above

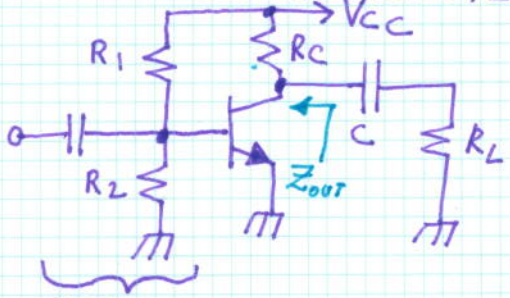
(8a) $\dfrac{\gamma}{r_C+r_E} = \dfrac{(1-\gamma)}{R_C+R_E}$

TELLS WHAT Q-POINT CENTERS THE AC-LOAD LINE PROPERLY

(8b) $\gamma_{centered} = \dfrac{1}{\left(\dfrac{R_C+R_E}{r_C+r_E}\right)+1}$

EQ. 8 SOLVED FOR $\gamma$

# MAXIMUM THEORETICAL EFFICIENCY – RC COUPLING




CIRCUIT CONFIGURATION

NOT INCLUDED – ASSUMED IDEAL

(1) $R_L = Z_{OUT} = R_C$

For maximum power transfer. Valid at relatively low frequencies where device impedance is largely resistive.

(2) $V_{pp} = 2 I_{c(Q)} r_c = 2 I_{c(Q)} \left(\frac{R_L}{2}\right) = 2 \frac{V_{CC}(1-\gamma)}{R_C + R_E} \cdot \left(\frac{R_L}{2}\right)$

Need to know $\gamma$. KNOW THAT $R_E \to 0$ and $r_E \to 0$ due to circuit layout.

From Eq (8b), $\gamma_{cent} = \frac{1}{\left(\frac{R_C + R_E}{r_C + r_E} + 1\right)} = \frac{1}{\left(\frac{R_C + 0}{\frac{R_L}{2} + 0} + 1\right)}$ and $R_C = R_L$

$$\gamma_{cent} = \frac{1}{\frac{R_L}{(R_L/2)} + 1} = \frac{1}{3}$$

(NON INTUITIVE RESULT TO MOST TECHNICIANS AND ENGINEERS!)

(2a) $V_{pp} = \frac{2 V_{CC}(1 - 1/3)}{R_L}\left(\frac{R_L}{2}\right) = \frac{2}{3} V_{CC}$

Best $V_{pp}$ signal out is 2/3 of $V_{CC}$!

(3) $P_{OUT} = \frac{V_{pp}^2}{8 R_L} = \frac{(2/3)^2 V_{CC}^2}{8 R_L}$

Best power out w/o clipping

(4) $P_{IN} = V_{CC} I_{c(Q)} = \frac{V_{CC}(V_{CC} - \gamma V_{CC})}{R_L}$

$R_C = R_{LOAD}$. Ignoring loss in base bias net. $\gamma = 1/3$

(4a) $P_{IN} = \frac{V_{CC}^2 (2/3)}{R_L}$

(5) $\eta_{MAX} = \frac{P_{OUT}}{P_{IN}} = \left(\frac{(2/3)^2 V_{CC}^2}{8 R_L}\right)\left(\frac{R_L}{V_{CC}^2 (2/3)}\right) = \frac{1}{12} = 0.08\overline{3} = 8.\overline{3}\,\%$